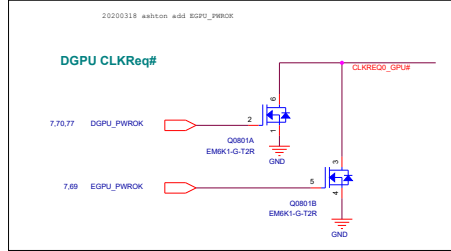




# CPU CLK



@20190624A

CLKREQ0\_GPU# -> CLKREQ0\_GPU#

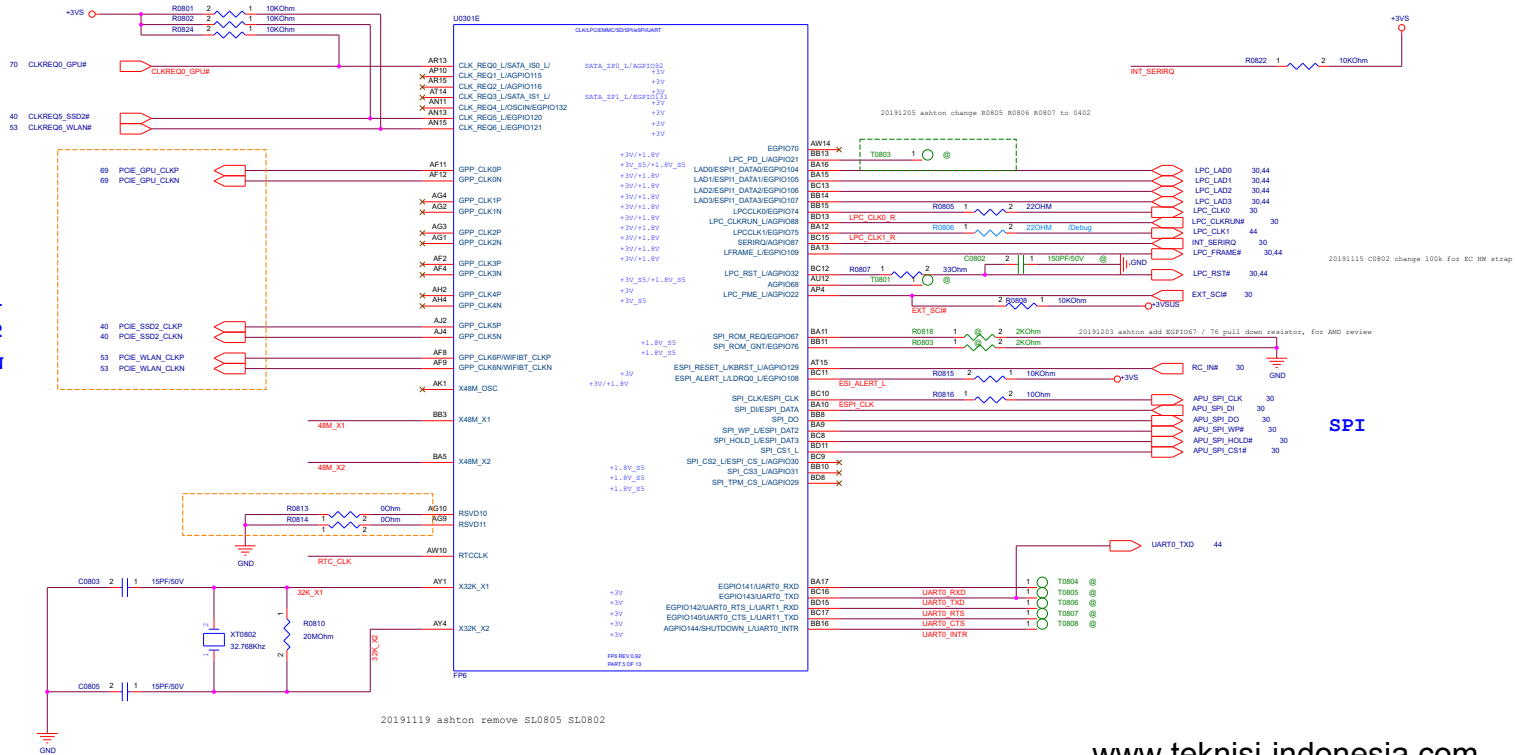
CLKREQ0\_SSD1# -> CLKREQ4\_SSD1#

CLKREQ3\_SSD2# -> CLKREQ5\_SSD2#

CLKREQ1\_WLAN# -> CLKREQ6\_WLAN#

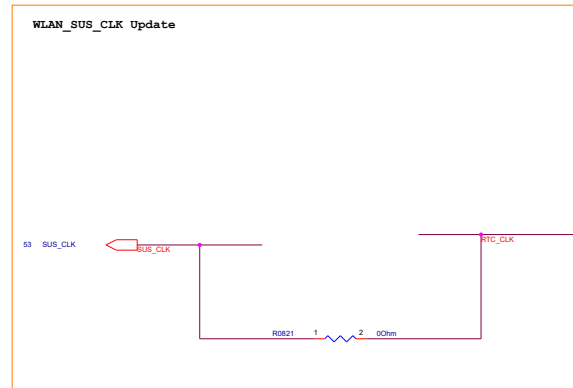
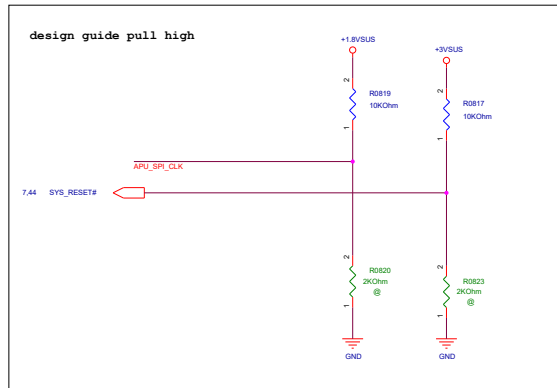
GPU  
CR1  
5G  
CR2  
SSD1  
SSD2  
WLAN

PCIE CLK P/N  
後端記得預留0 ohm



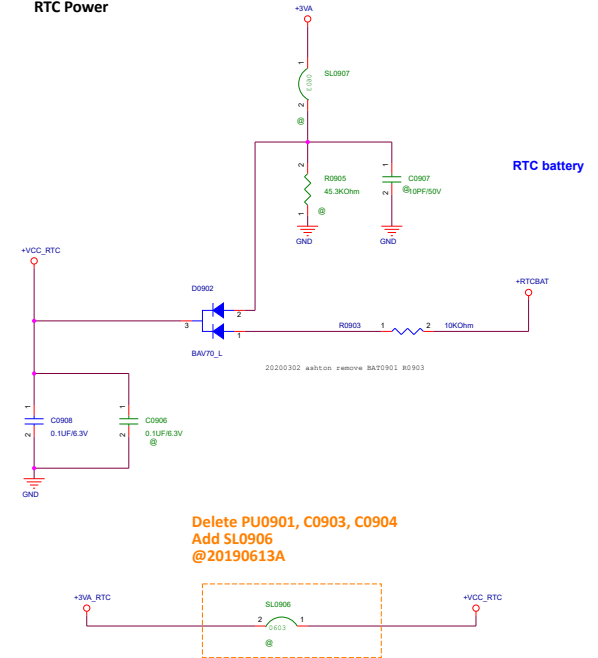
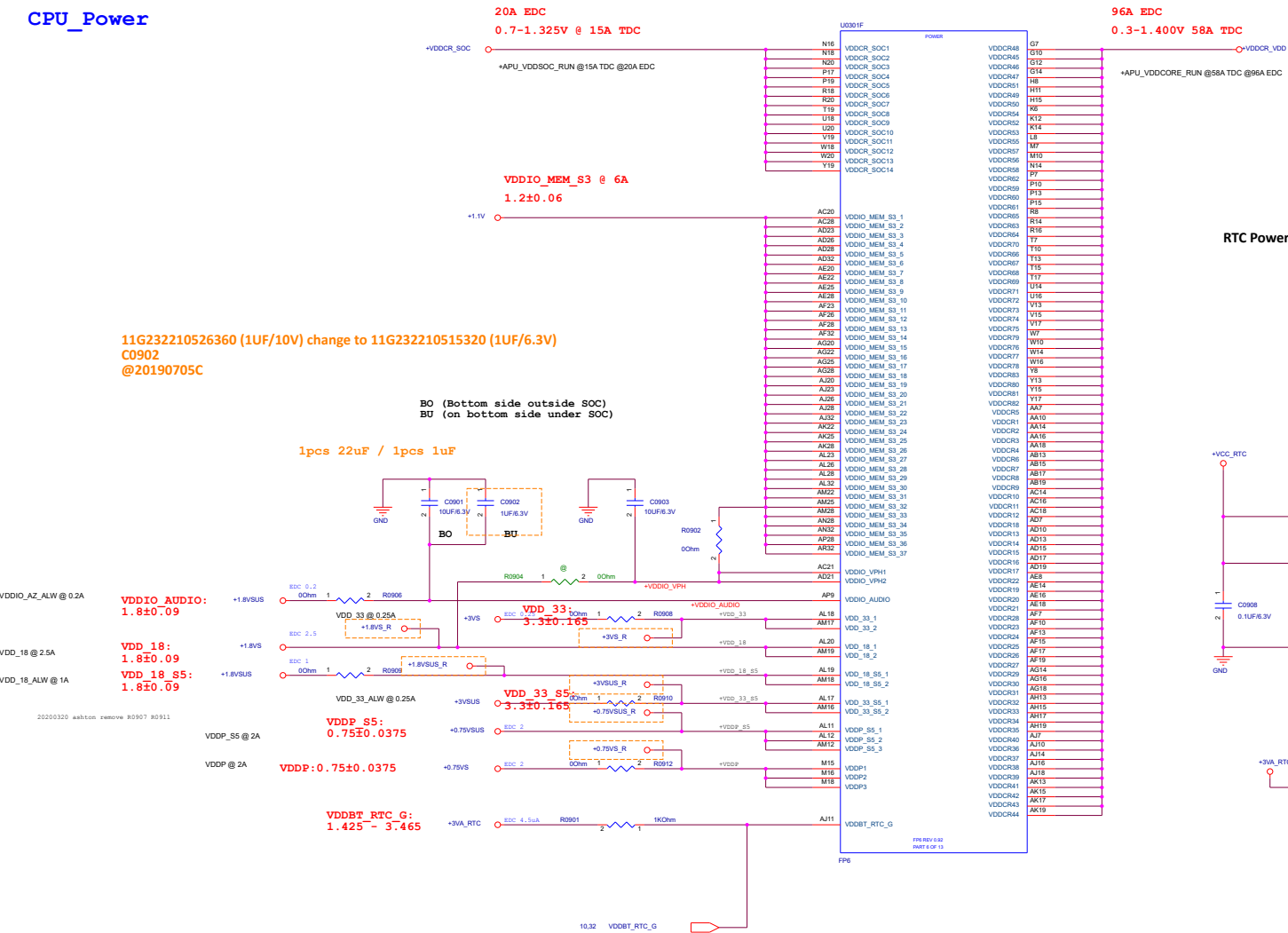
SPI

www.teknisi-indonesia.com



<<Variant Name>>

## CPU\_Power



<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

Date:


Tuesday, December 01, 2020

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		Project Name	Rev
		GX502GX	R1.2
Title : CYPRESS CCG4			
Size	Dept.: ASUSTek COMPUTER INC Engineer: NR EE RD3		
B			
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<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

R1.0

Date:

Tuesday, December 01, 2020

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Project Name

**GX531GX**

Rev

1.0

**Title :** **DIM\_DDR4 SO-DIMM B1**

Size

A

**Dept.:** **ASUSTeK COMPUTER INC. NB1** **Engineer:** **NR EE RD3**

Date: **Tuesday, December 01, 2020**

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<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

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Tuesday, December 01, 2020

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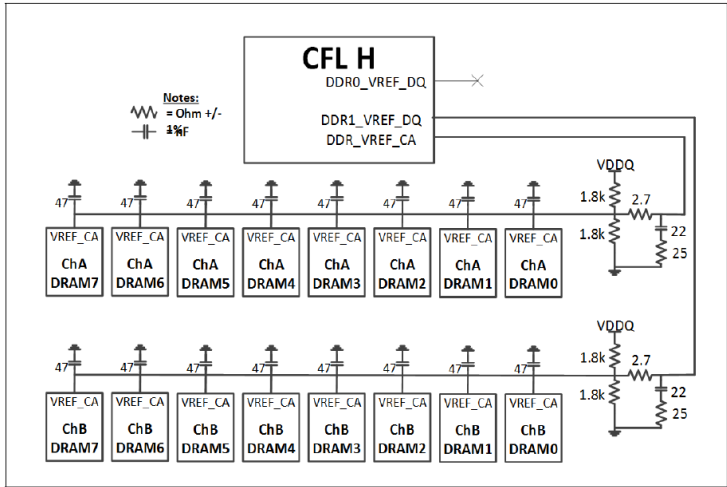
17

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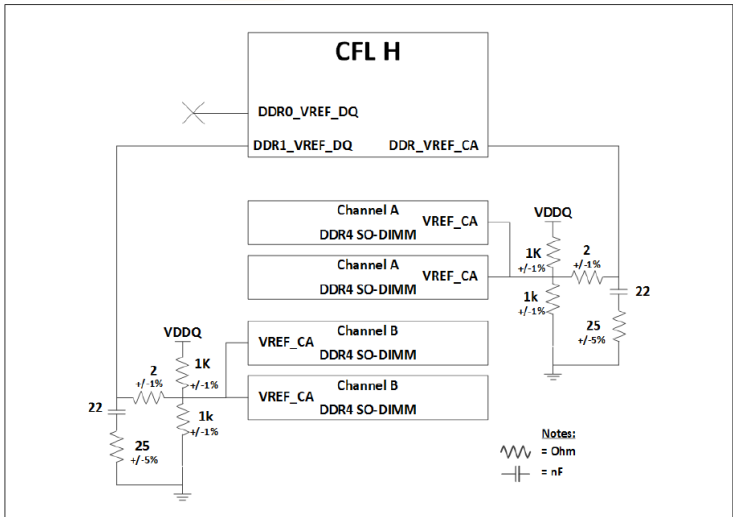


Figure 4-24. CFL-H DDR4 x8 Memory Down V<sub>REF-CA</sub> Overview




Memory Down Vref

Figure 4-22. CFL-H DDR4 SO-DIMM V<sub>REF-CA</sub> Overview



SO-DIMM1 Vref

		<b>Title :</b> <b>DDR4_TERMINATION</b>	
<b>ASUSTeK COMPUTER INC.</b>		<b>Engineer:</b> <b>NR EE RD3</b>	
<b>Size</b> <b>A</b>	<b>Project Name</b> <b>GX531GX</b>		<b>Rev</b> <b>1.0</b>
<b>Date:</b> <b>Tuesday, December 01, 2020</b>		<b>Sheet</b> <b>19</b> <b>of</b> <b>104</b>	

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20191121 ASHTON change USB2.0 port  
 , USBC0 for USB port A, USBC4 for  
 USBC portB, USB5 for typeA

USB3.0 TX/RX  
 I/O-IOVPS5-D\_VDDP (S5\_0.75)\_FP6 (FDS)

USB Port0 Type-C Port0

USB Port2 N-KEY

USB Port3 BT

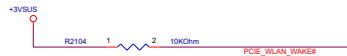
USB Port4 Type-C Port4

USB Port5 Type-A Port5

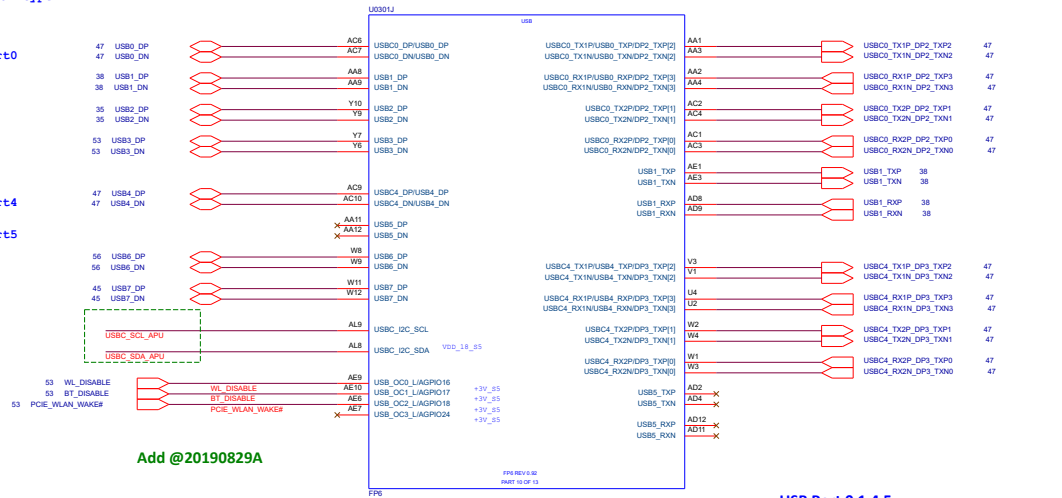
USB Port6 FP

AMD Design check

AGPIO13. If unused, enable internal pull down by software.



Add @20190829A



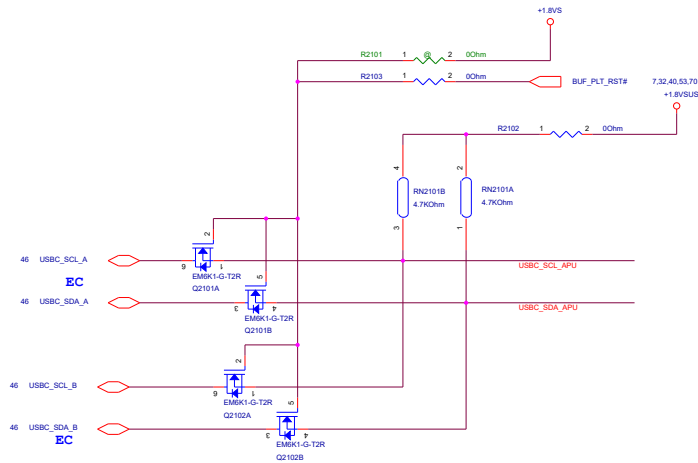
USB3.1 Gen2 USB-C Poart A

USB3.1 Gen2 Type-A

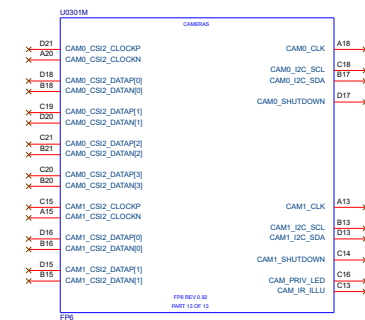
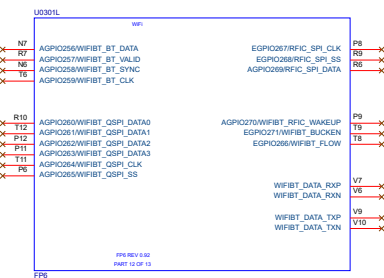
USB3.1 Gen2 USB-C Poart B

USB3.1 Gen2 Docking

USBC\_SDA/SCL level shift change +1.8VS  
 20200901 ashton modify



USB Port 0,1,4,5  
 USB-A USB3.2 Gen1(5Gbps): 304.8mm (12000mil)  
 USB-C USB3.2 Gen1(5Gbps): 177.8mm (7000mil)  
 USB-A & USB-C USB3.2 Gen2(10Gbps): 152.4mm (6000mil)



<Variant Name>

ASUS Project Name  
 Title : FX505DY Rev R1.0

Size Dept.: NB-SZ-RD3 Engineer: Date: Tuesday, December 01, 2020 Sheet 21 of 104

<Variant Name>

Title

<Title>

Size

A

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<RevCode>

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Title

<Title>

Size

A

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Rev

<RevCode>

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<Title>

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<RevCode>

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<Variant Name>

Title

<Title>

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A

Document Number

<Doc>

Rev

<RevCode>

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<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

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<Variant Name>

Title

<Title>

Size

A

Document Number

GA401

Rev

<RevCode>

Date:

Tuesday, December 01, 2020

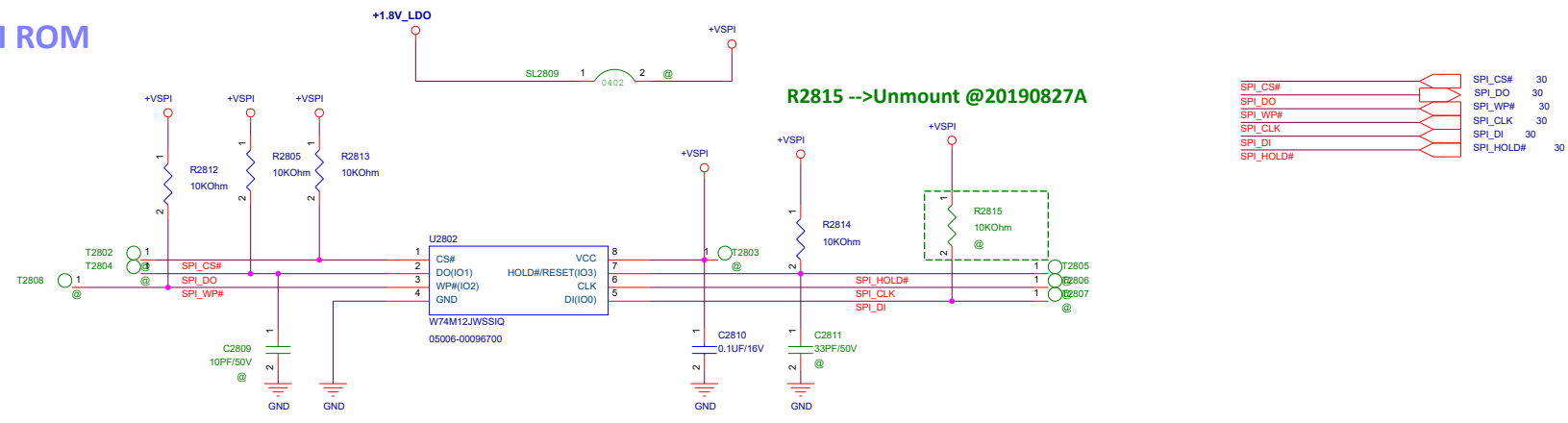
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## SPI ROM

+3VA\_EC

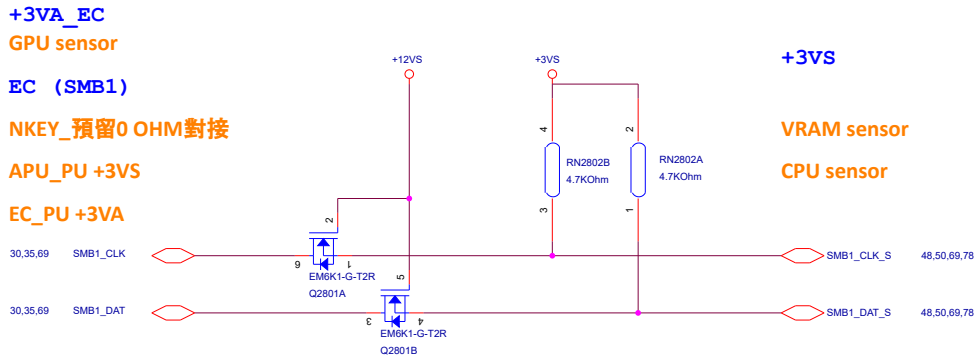
## GPU sensor

EC (SMB1)

## NKEY\_預留0 OHM對接

APU\_PU +3VS

EC\_PU +3VA



+3VA\_EC

## SEC (SMB3)

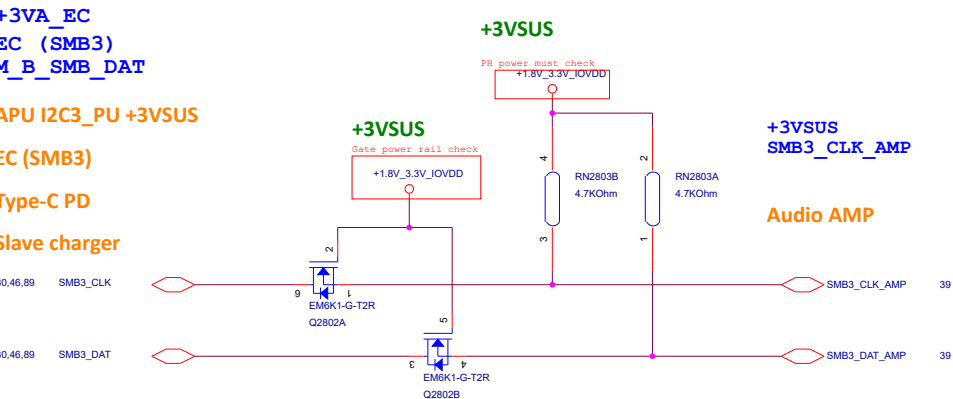
M\_B\_SMB\_DAT

APU I2C3\_PU +3VSUS

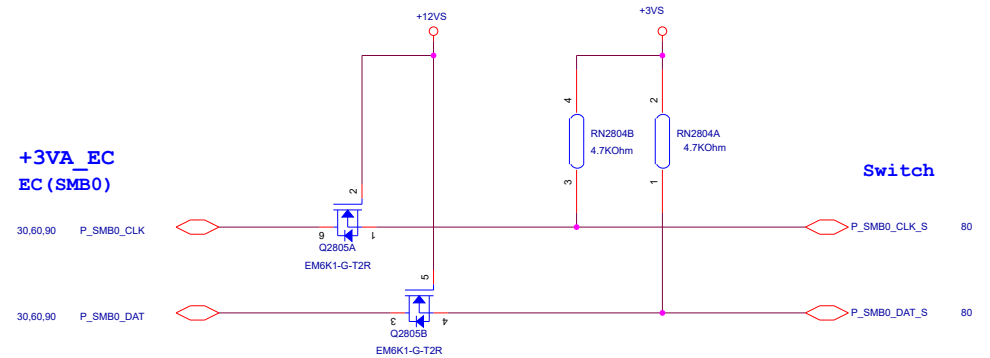
## EC (SMB3)

## Type-C PD

## Slave charger

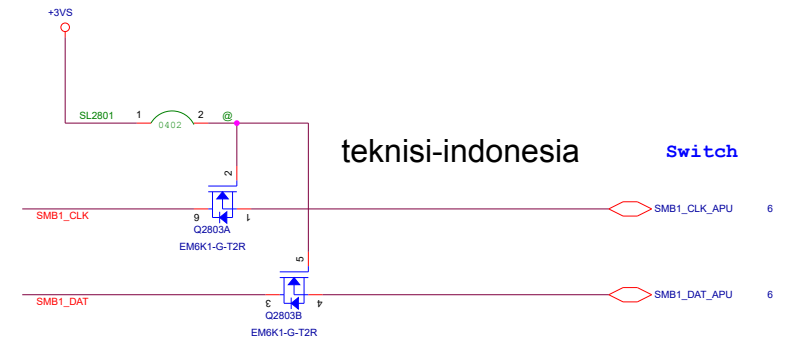
 $+3V_{A\_EC}$ 

EC (SMB0)



teknisi-indonesia

## Switch



<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

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Tuesday, December 01, 2020

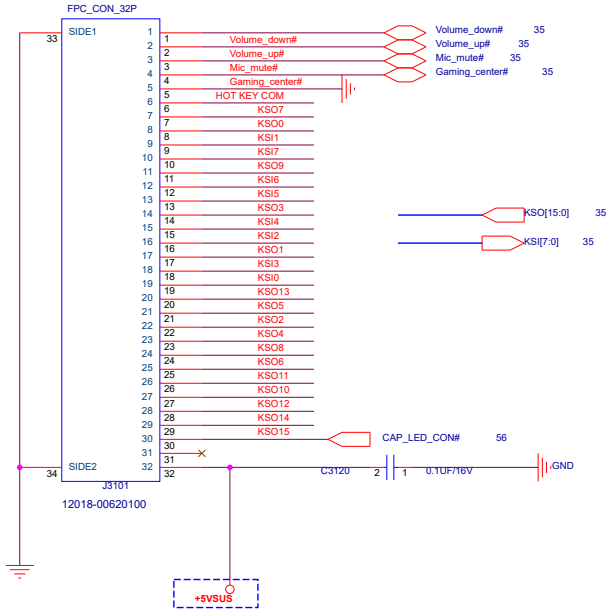
Sheet

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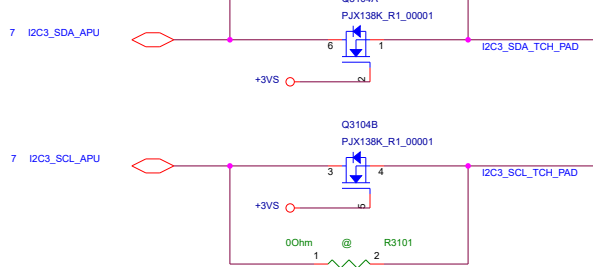
of

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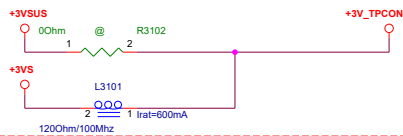
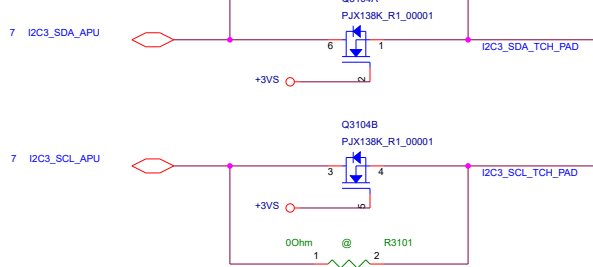
12018-00620100



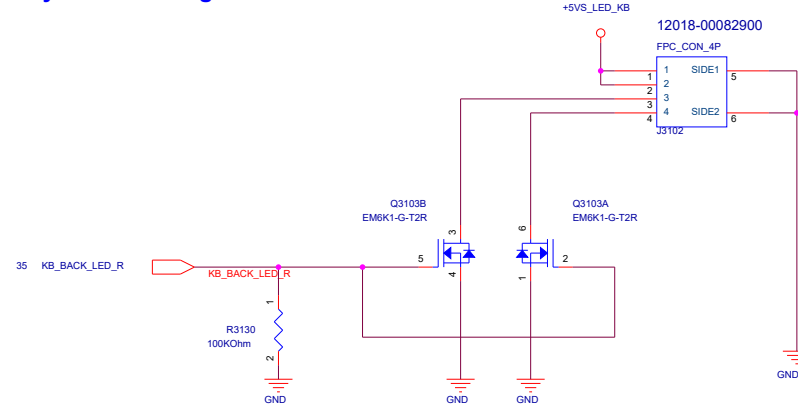
PU +3VSUS



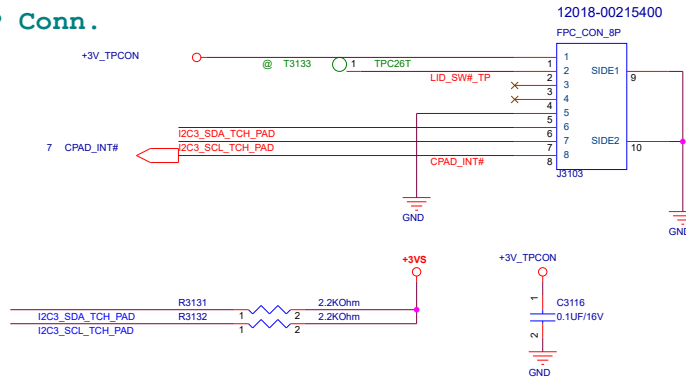
PU +3VS



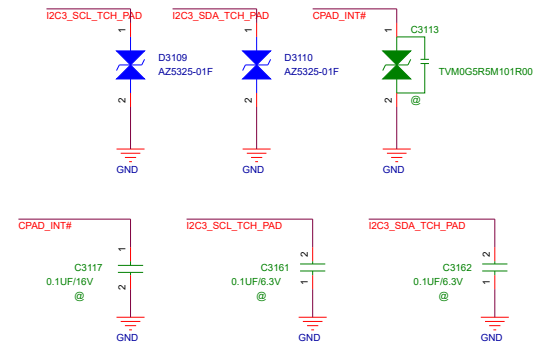
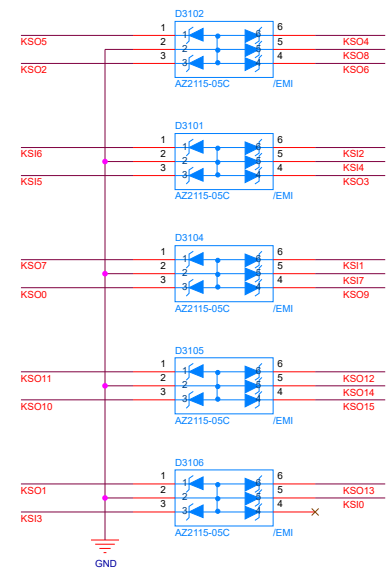
## Keyboard Backlight CON.



## TP Conn.

EMI Reserve  
如上件確認容值(選Pico級)

for ESD

For EMI  
20170411 ashton modify

&lt;Variant Name&gt;

ASUS		Title : KBC_KB & TP	
ASUSTek COMPUTER		Engineer: NR EE RD3	
Size	Project Name	GM501	
B		Rev R1.0	
Date: Tuesday, December 01, 2020	Sheet	31	of 104





Project Name

**GU502DU**

Rev

**R1.0**

**Title :** **LAN RTL8111GUX-CG**

Size

**B**

**Dept.:**

**ASUSTeK COMPUTER INC. NB1**

**Engineer:**

**NR EE RD3**

Date: **Tuesday, December 01, 2020**

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**104**





Project Name

**GU502DU**

Rev

**1.0**

**Title :**      **LAN\_RJ45\_CON**

Size

**B**

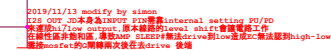
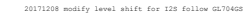
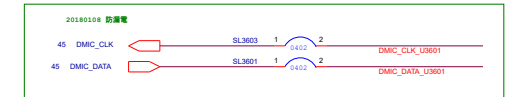
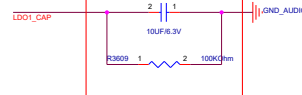
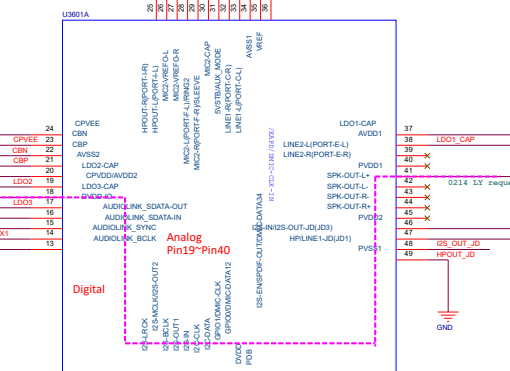
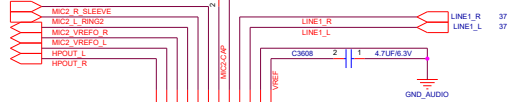
**Dept.:**      **ASUSTeK COMPUTER**

**Engineer:**      **NR EE RD3**

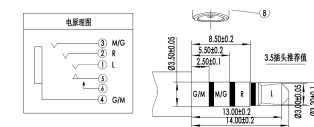
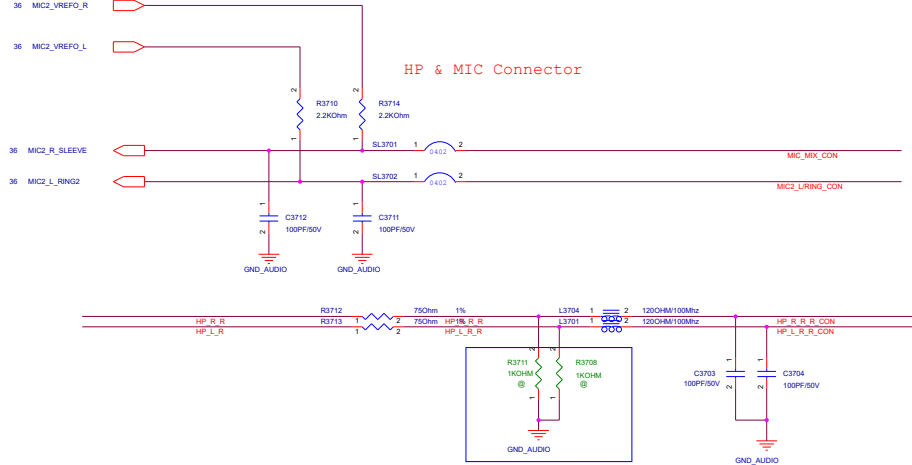
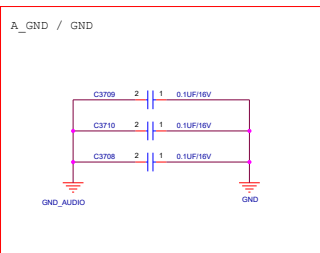
Date: **Tuesday, December 01, 2020**

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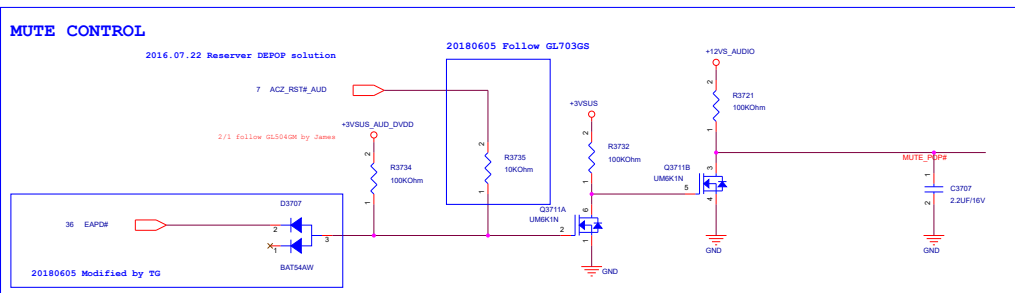
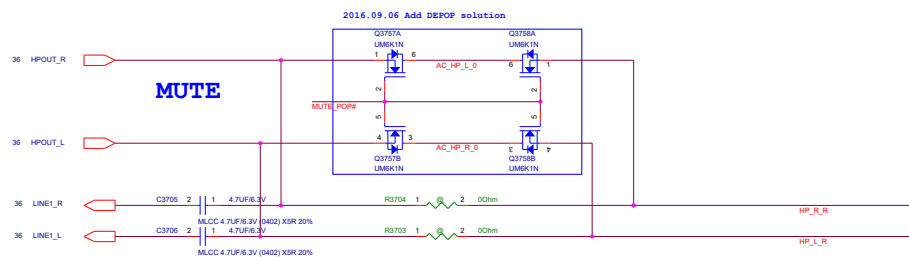
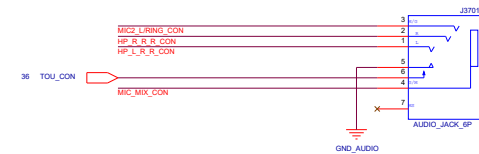
[illegible]



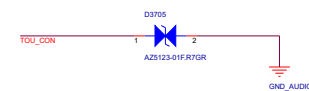
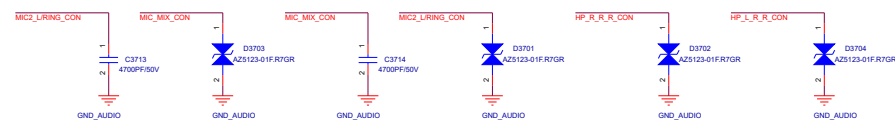
A\_GND / GND



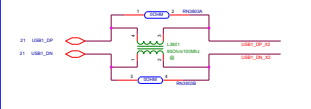
## HP & MIC Connector



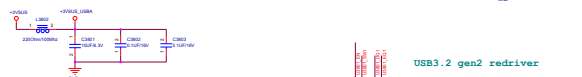
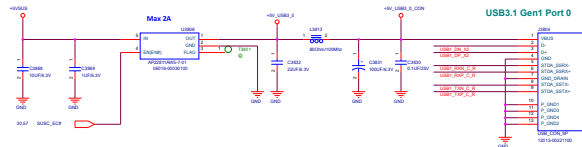
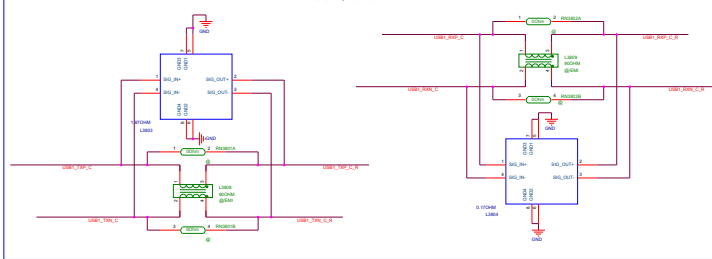
## EMI



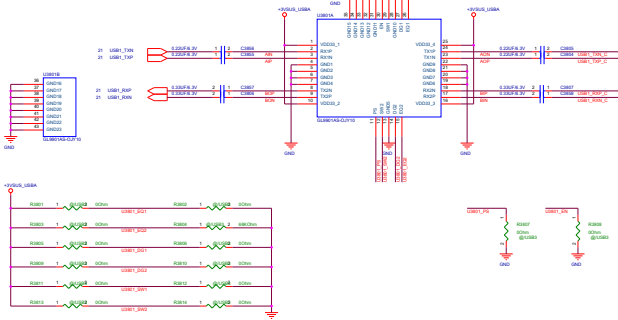
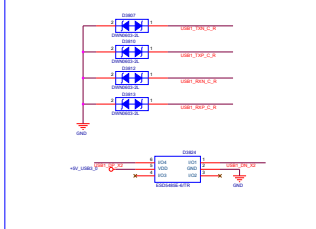
## USB2.0 EMI-Protection



## USB3.0 EMI-Protection



## ESD-Protection



©2019 ASUSTeK Computer Inc.

Title: Asul HP Jack, MIC

Engineer: NW EE RD3

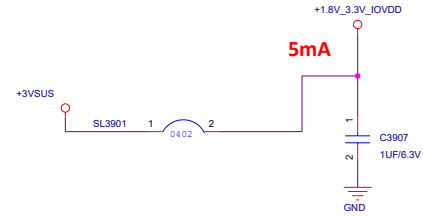
Rev: 1.0

## SPK Power



## IO Power

20191216 ashton remove R3907 reserve +1.8VSDUS



## INTERNAL SPK1 Conn.

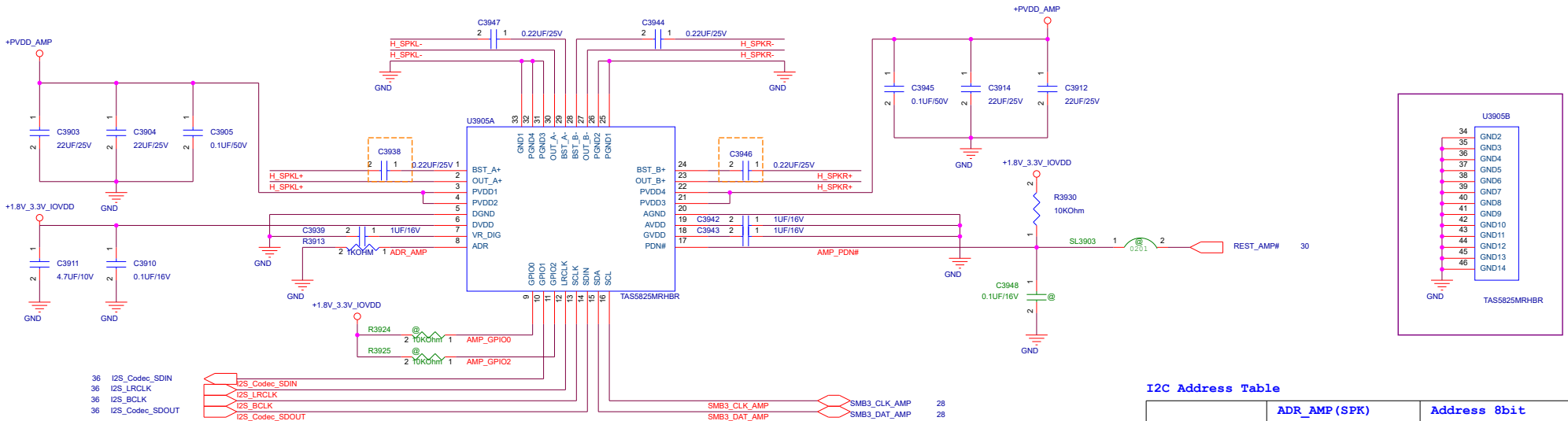
SPK L+ L- R+ R- trace width

Speaker 8 ohm

Max = 1.5W / Channel

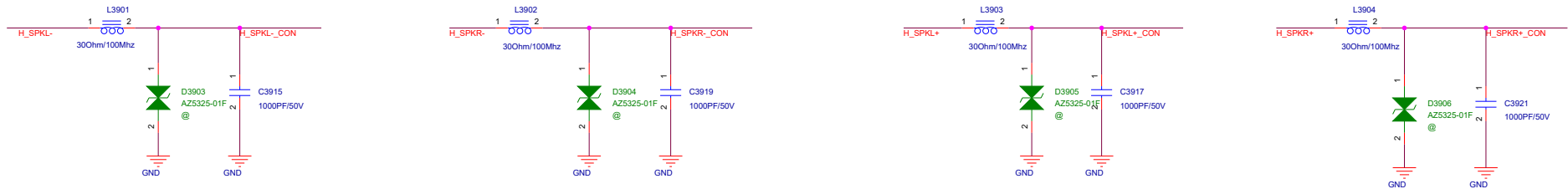
I = 0.43 A

(Smart AMP MAX 2A/Channel) ==> 60mils



Modify @20181017A

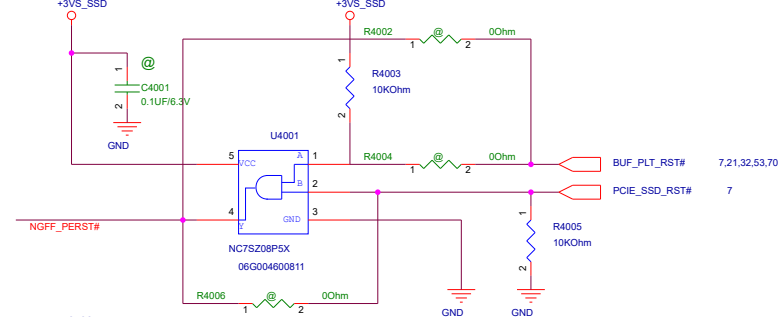
## SPK Output



## I2C Address Table

	ADR_AMP (SPK)	Address 8bit
Main(N.C.)	Open	0x9A
Second	Short	0x98




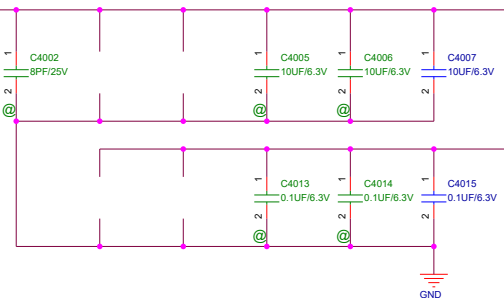


+3VS\_SSD

1

2

R4001  
10KOhm




H4001  
CT236CB176D146  
13020-05070100







		<b>Title :</b> <b>NGFF_SSD_CPU</b>	
<b>ASUSTeK COMPUTER</b>		<b>Engineer:</b> <b>NR EE RD3</b>	
<b>Size</b>  <b>A</b>	<b>Project Name</b>  <b>GX502GX</b>		<b>Rev</b>  <b>1.0</b>
<b>Date:</b> <b>Tuesday, December 01, 2020</b>		<b>Sheet</b> <b>41</b> of <b>104</b>	



Project Name

**GZ701GX**

Rev

R1.0

**Title :** **CR\_GL9750 colay GL9760**

Size

A

**Dept.:** **ASUSTeK COMPUTER INC. NB1** **Engineer:** **NR EE RD3**

Date: **Tuesday, December 01, 2020**

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Project Name

**GX502GX**

Rev

**1.0**

**Title :**      **CB\_CON**

Size

**A**

**Dept.:**      **ASUSTeK COMPUTER**

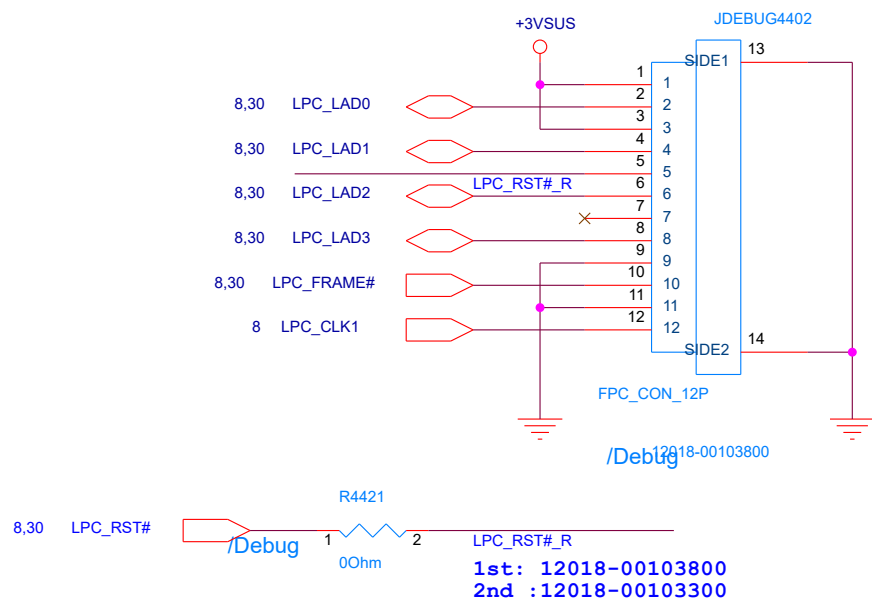
**Engineer:**      **NR EE RD3**

Date: **Tuesday, December 01, 2020**

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LPC Debug Port

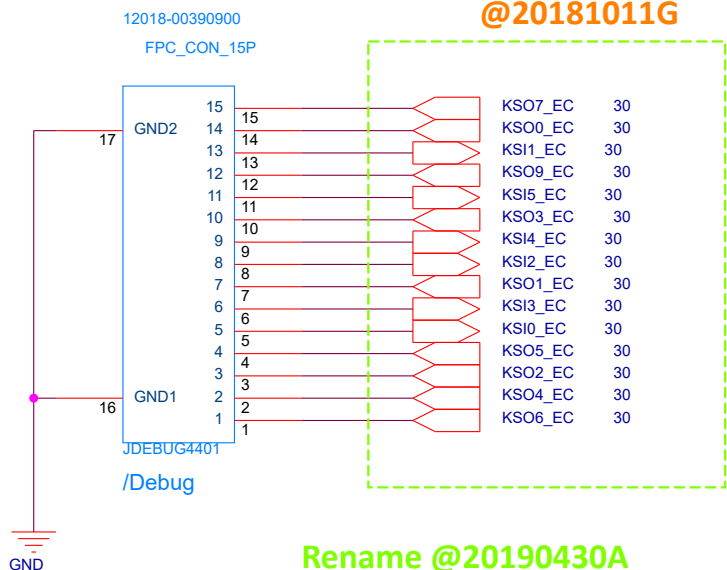
2017/11/10



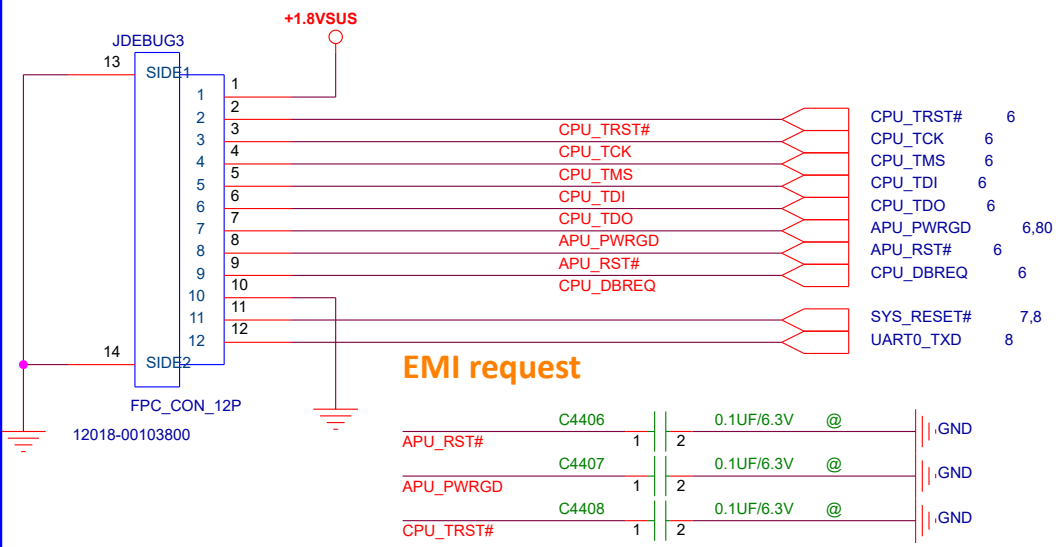
2017/11/10

Flash BIOS


Rename  
@20181011G



HDT + UART Debug



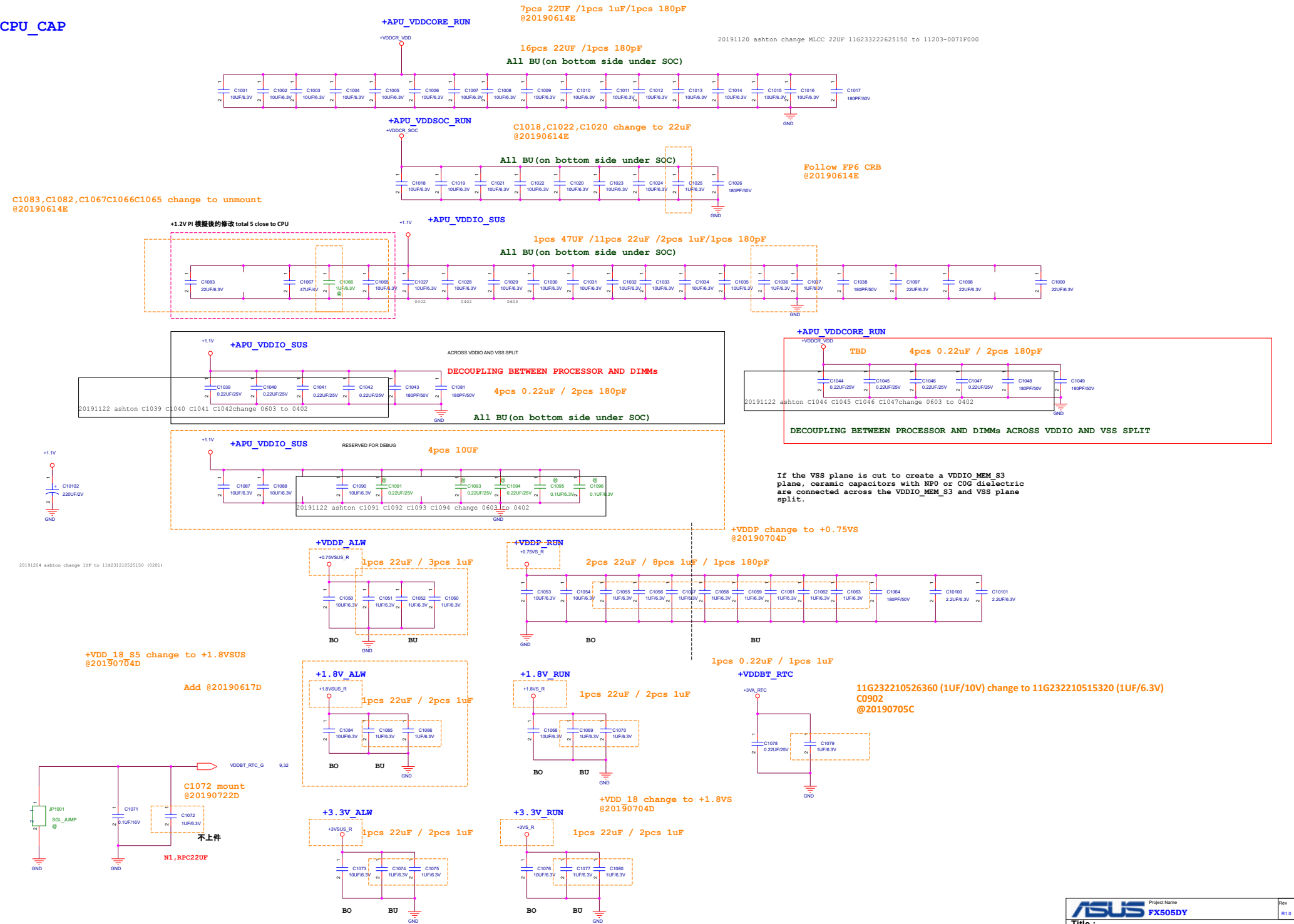
<Core Design>

		Title : <b>DEBUG_LPC</b>	
ASUSTek COMPUTER		Engineer: <b>NR EE RD3</b>	
Size <b>A</b>	Project Name <b>GX502GX</b>		Rev <b>1.0</b>
Date: <b>Tuesday, December 01, 2020</b>		Sheet <b>44</b> of <b>104</b>	






CPU\_CAP





		Project Name		Rev
		<b>GX502GX</b>		1.0
Title : <b>ANT</b>				
Size  B	Dept.: <b>ASUSTeK COMPUTER</b>		Engineer:	<b>NR EE RD3</b>
Date: <b>Tuesday, December 01, 2020</b>			Sheet	<b>49</b> of <b>104</b>

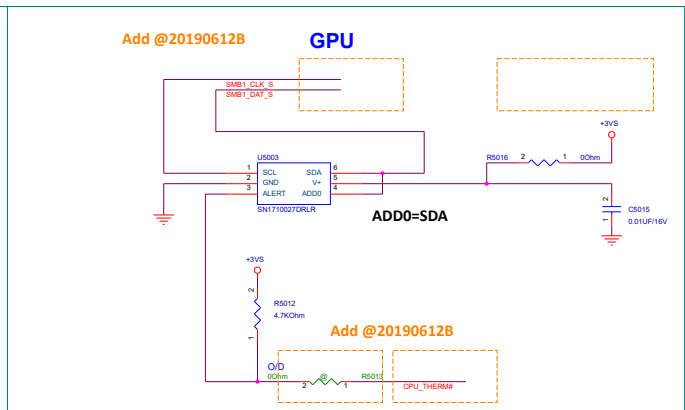
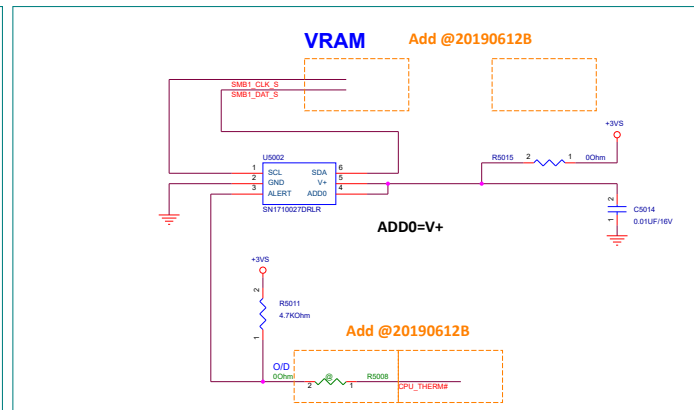
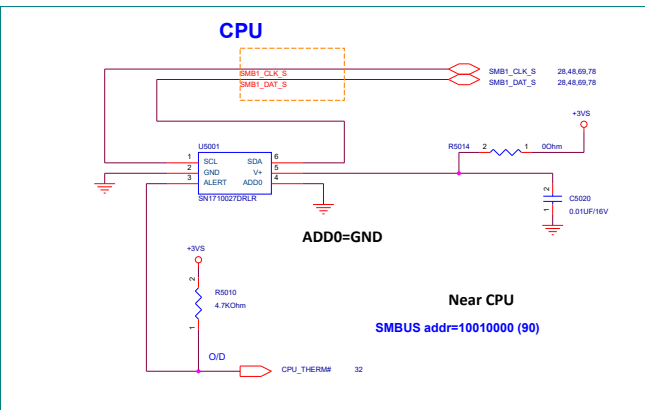
# Thermal Sensor : SN1710027

ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

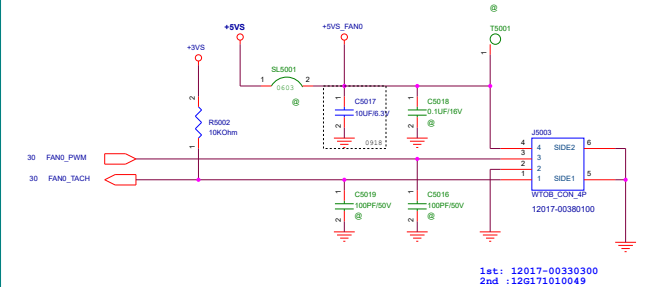
Pin function Supply voltage.: 1.62 V to 3.6 V

power rail : 3.3V

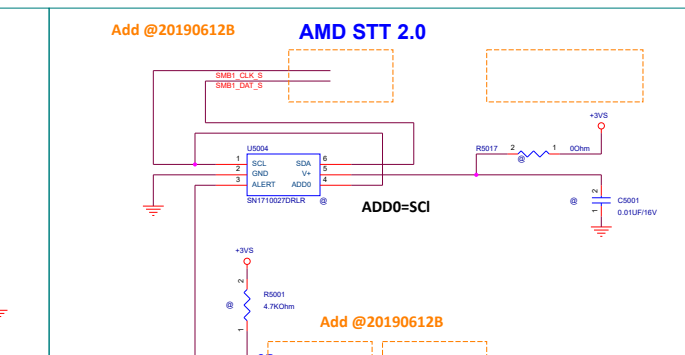
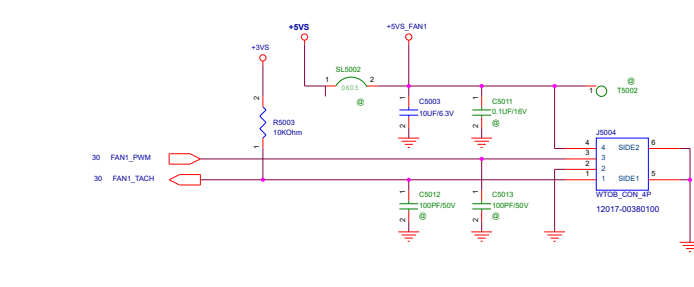
SMBUS1 to EC



## CPU&GPU FAN



Note : connector and power are by project design

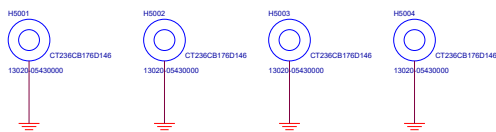


TBD

SMBUS addr=10010010 (92)

ADD0: Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION	Output
1001000 90	Ground	CPU
1001001 91	V+	VRAM
1001010 92	SDA	GPU
1001011 93	SCL	



<Core Design>



**Title :** TYPE-C USB3.1\_R1.5\_4

ASUSTeK COMPUTER

**Engineer:**

Size

Project Name

Rev

A

**GX502GX**

1.0

Date: Tuesday, December 01, 2020

Sheet 51 of 104



**Title :** TYPE-C USB3.1\_R1.5\_4

ASUSTeK COMPUTER

**Engineer:**

Size

Project Name

Rev

A

**GX502GX**

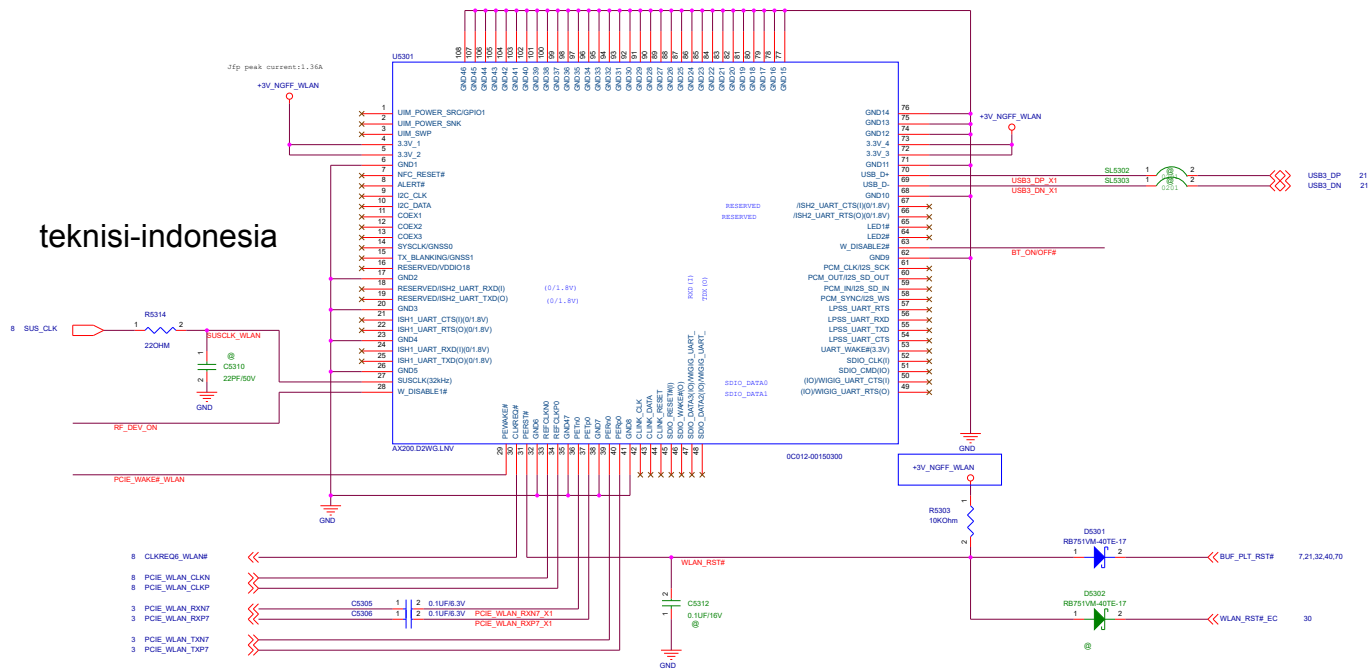
1.0

Date: Tuesday, December 01, 2020

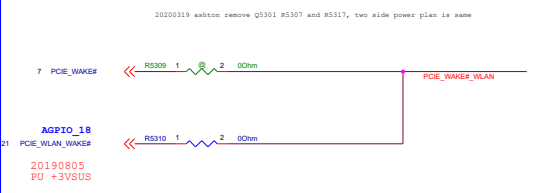
Sheet 52 of 104

## WLAN\_Intel\_AX200

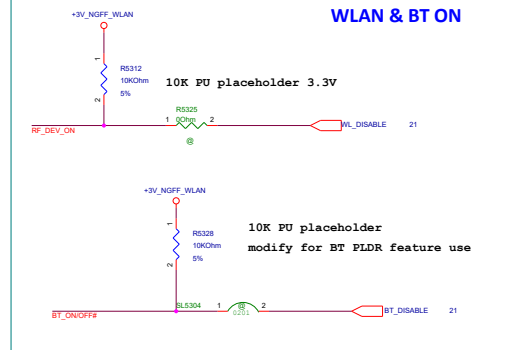
teknisi-indonesia



## WLAN\_Wake# Control



## WLAN &amp; BT ON





Project Name

**IP2021**

Rev

R1.0

**Title :** **5G\_mmWave**

Size

A

**Dept.:**

ASUSTeK COMPUTER INC. NB1

**Engineer:**

**NR EE RD3**

Date: **Tuesday, December 01, 2020**

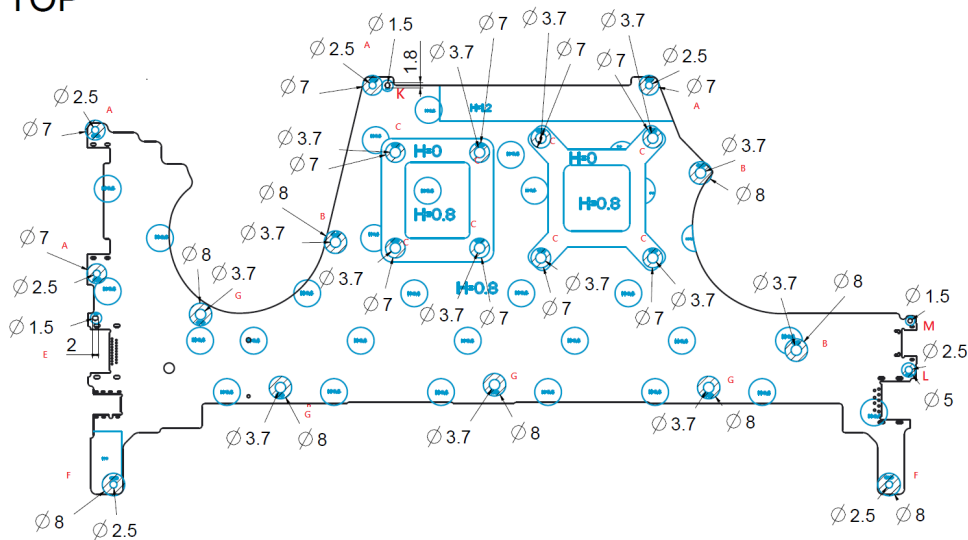
Sheet

**54**

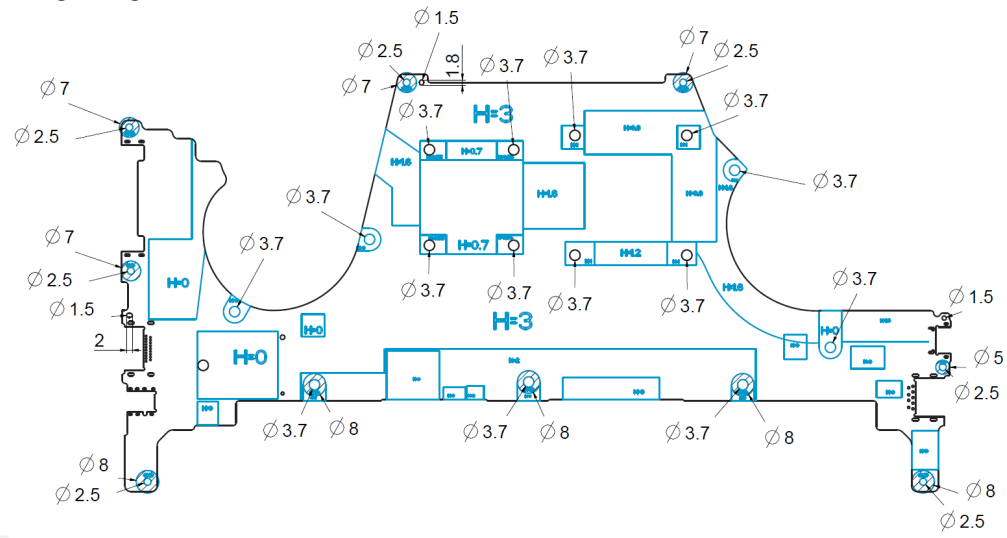
of

**104**

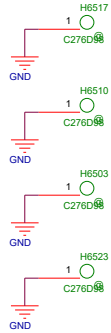
TOP



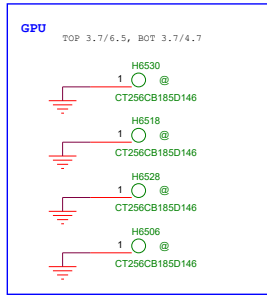
BOTTOM



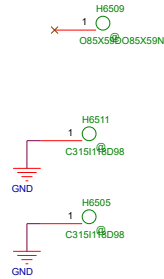
A



C &amp; D



E

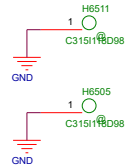


H

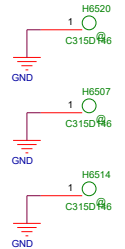
20200324 H is SSD nut at Page40

I

F

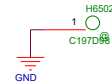


G

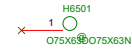


J

L



K




B

20200324 B is FAN nut at Page50


**CPU** TOP 3.7/6.5, BOT 3.7/4.7


&lt;Core Design&gt;

<b>ASUS</b>		Title : I/O board FUNC key	
ASUSTeK COMPUTER		Engineer: NR EE RD3	
Size B	Project Name GX502GX	Rev 1.0	
Date: Tuesday, December 01, 2020	Sheet	65	of 104

		Project Name <b>UX562FA_TP</b>		Rev  R2.0
<b>Title :</b> <b>Touch Panel Control block</b>				
Size  A	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC. NB1</b> <b>Engineer:</b> <b>EE</b>			
Date: <b>Tuesday, December 01, 2020</b>			Sheet <b>66</b>	of <b>104</b>



		<b>Title :</b> ME_Screw Hole & Nut	
ASUSTeK COMPUTER		<b>Engineer:</b> NR EE RD3	
Size  A	Project Name  <b>GX502GX</b>		Rev  1.0
Date: Tuesday, December 01, 2020		Sheet 67 of 104	

		<b>Title :</b> OTH_for test only	
ASUSTeK COMPUTER		<b>Engineer:</b> NR EE RD3	
Size  A	Project Name  GX502GX		Rev  1.0
Date: Tuesday, December 01, 2020		Sheet 68 of 104	







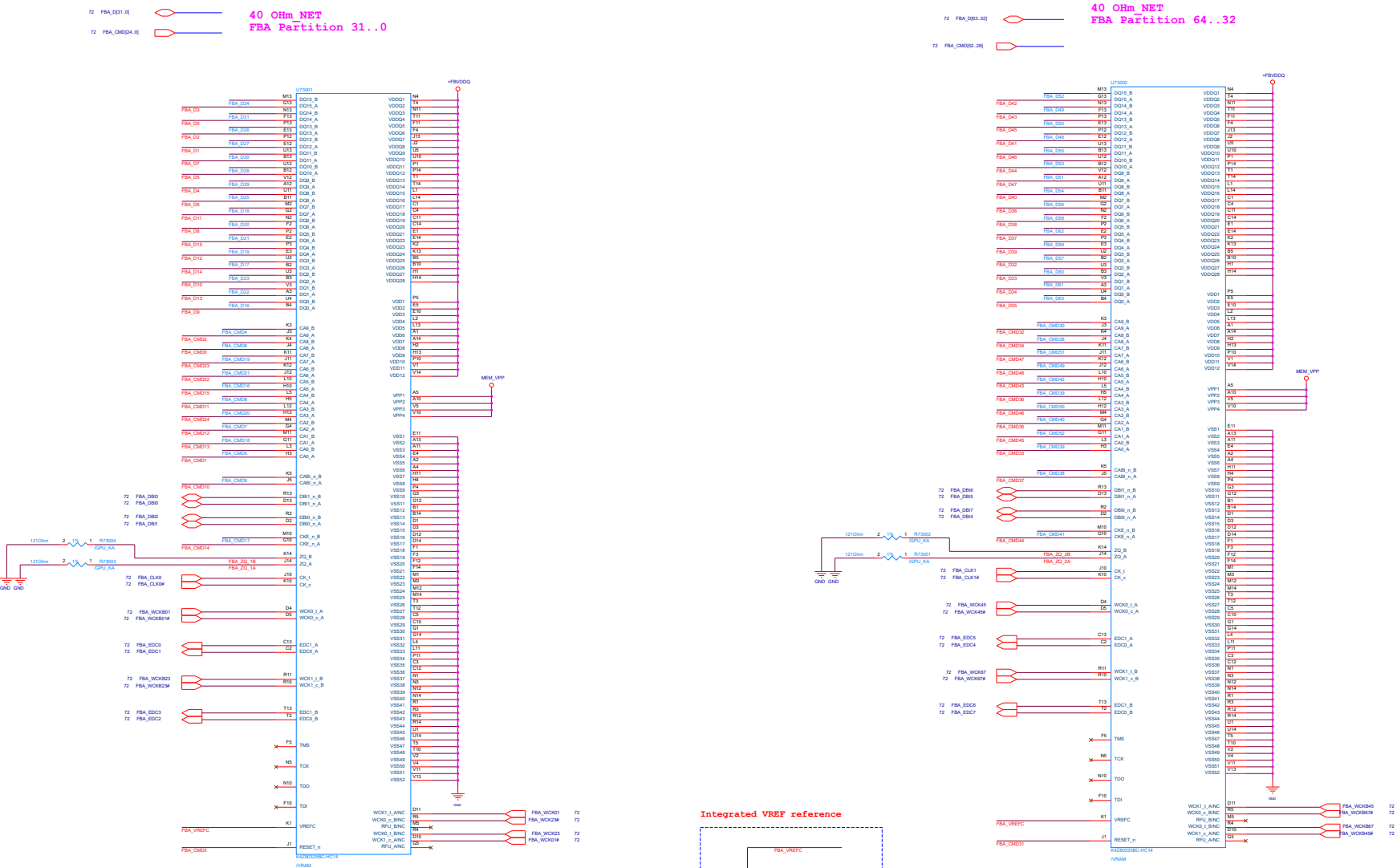


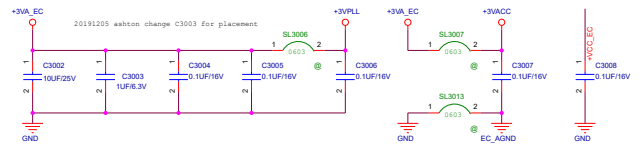
Table 4. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	Yes, TBD <sup>1</sup>	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	Yes, TBD <sup>2</sup>	Full	Production candidate

## Notes:

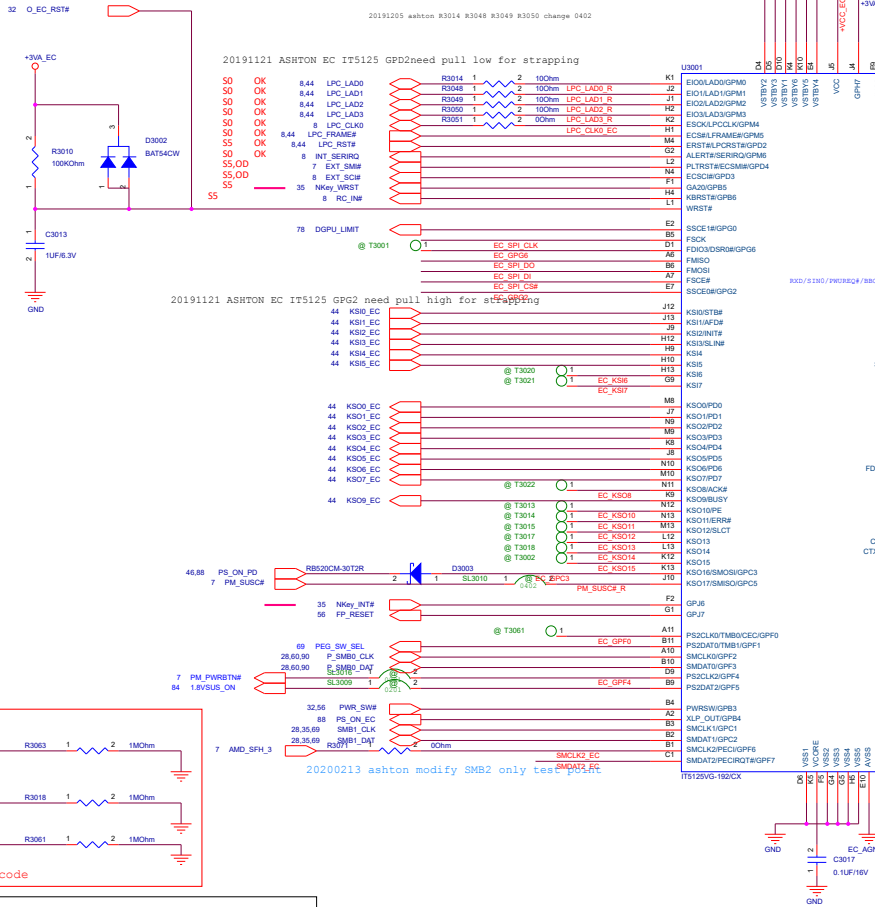
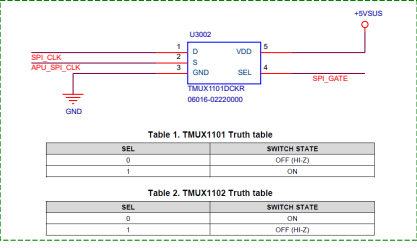
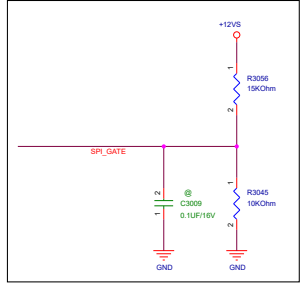
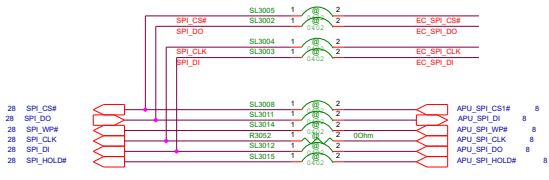
- For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
- Requires Production GDDR6 with a specific date code restriction. Exact date code is currently TBD.

## EC Power



VCC => +3VS system power ; LPC  
VSTBY=>+3VA\_EC ; Power supply of EC power

## Short Land & 0 ohm



+3VACC==+3VA\_EC,  
+3VAPLL==+3VA\_EC,0906

CON SW1\_DET add PD  
20200818 ashton modify

LPC\_CLKRUN# OD, LPC Power Rail +3VS

DEEP\_S3

PD\_IIN ID

PM\_RSMRST#

PM\_PWROK

PM\_PWROK

PM\_PWROK

PM\_PWROK

PM\_PWROK

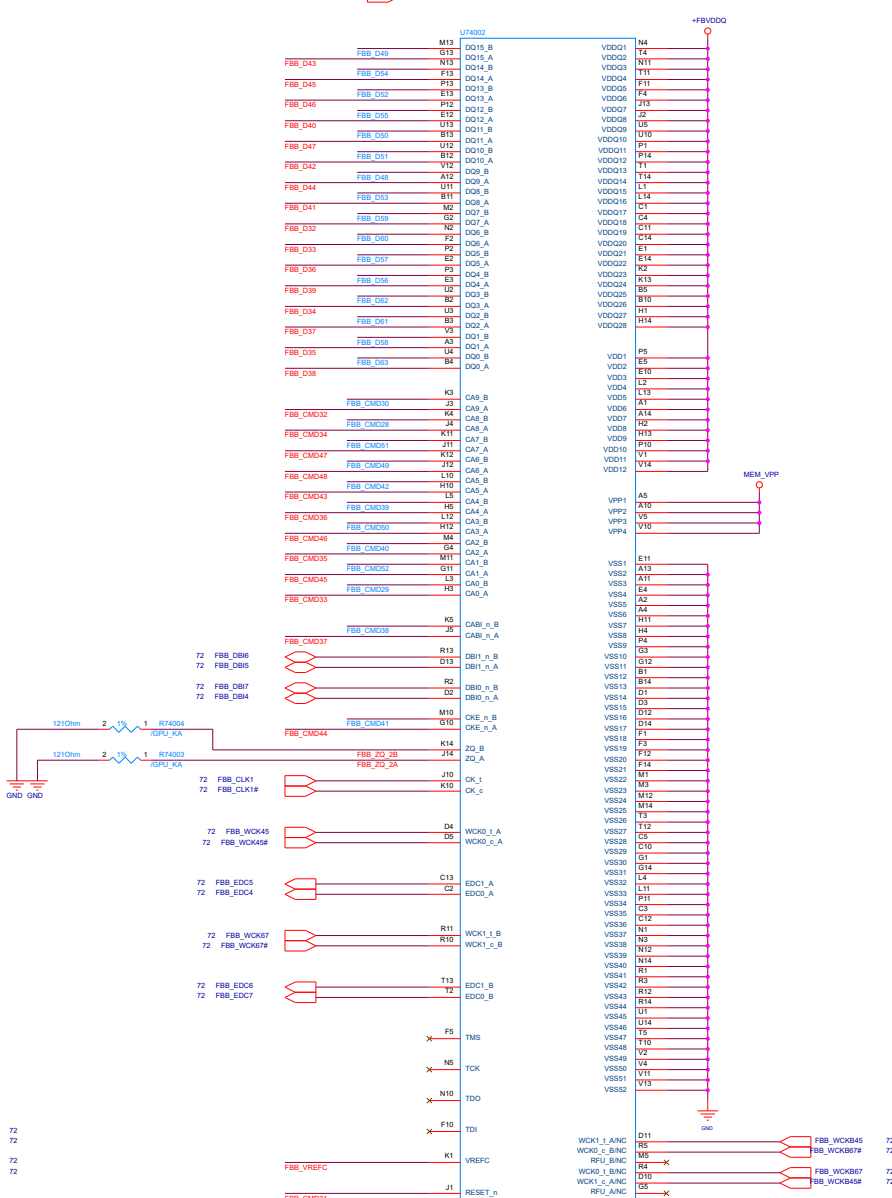
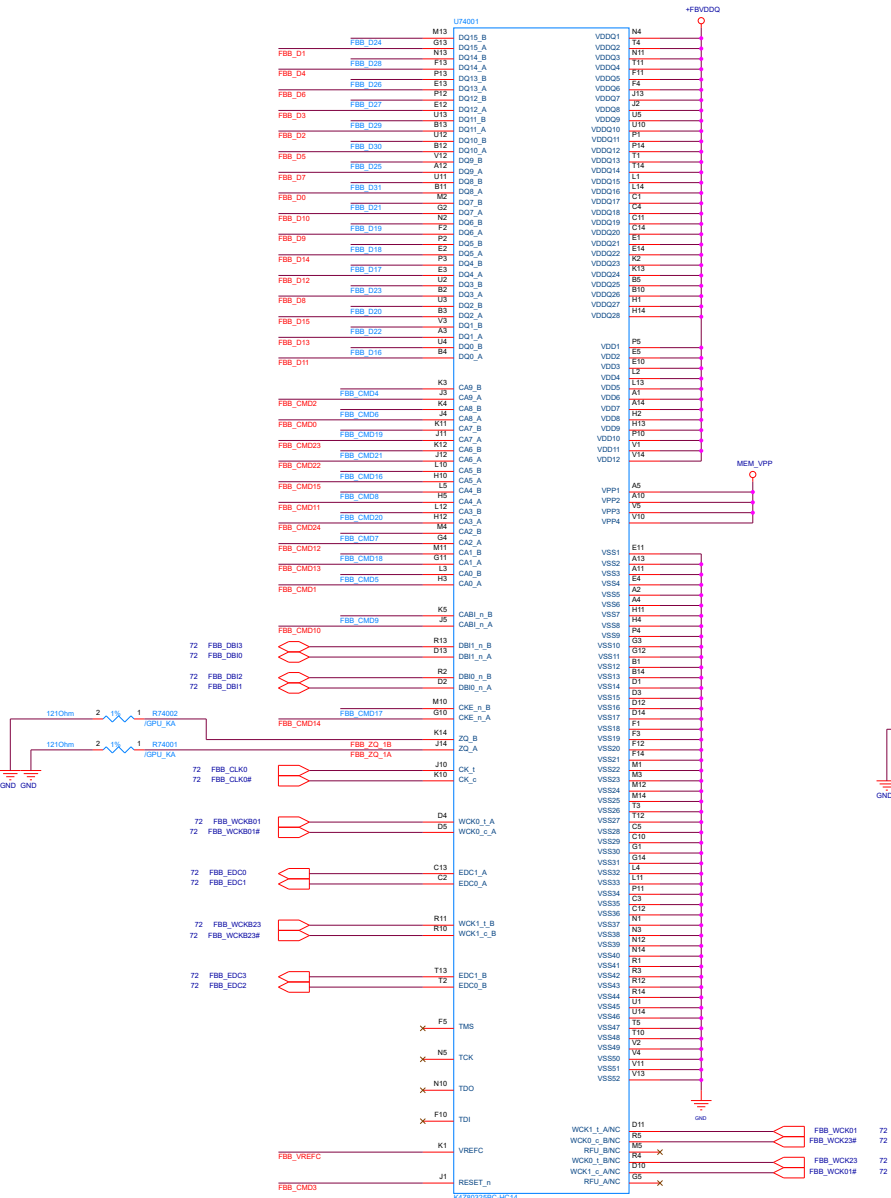
PM\_PWROK

PM\_PWROK

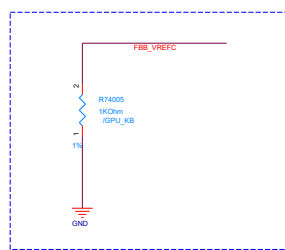
PM\_PWROK

PM\_PWROK

PM\_PWROK



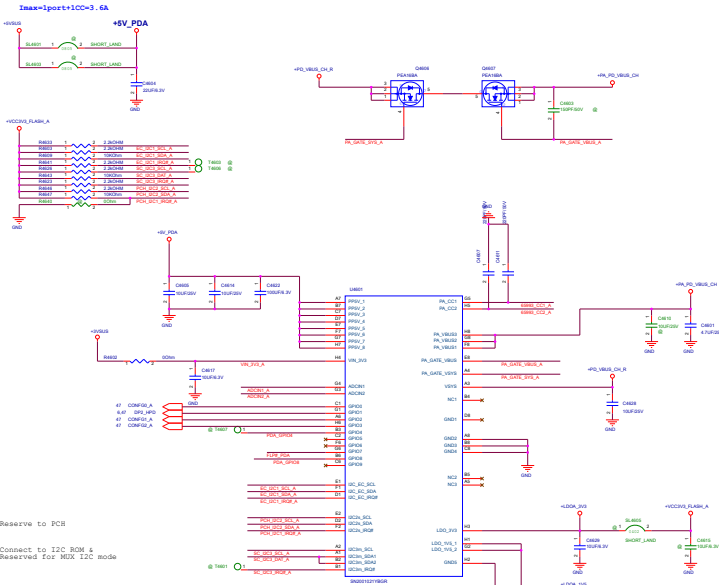
Integrated VREF reference



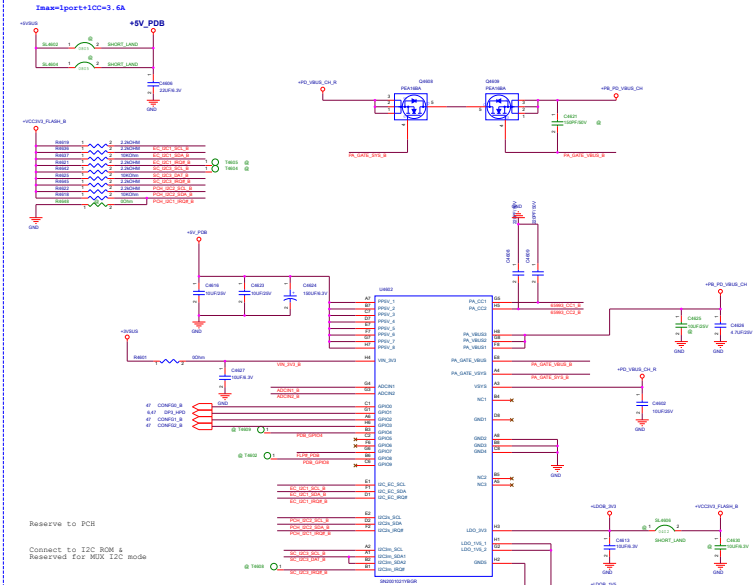
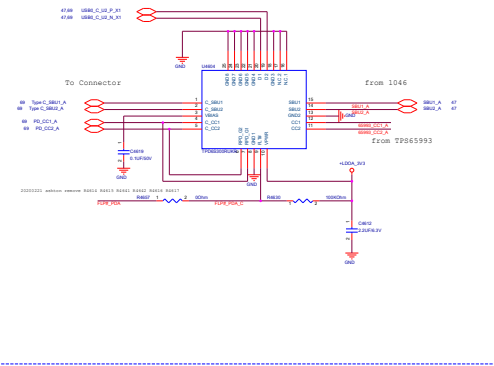
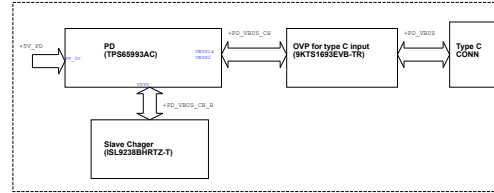
<Variant Name>

File	<File>	Rev	R1.0
Size	Document Number		
C	G512L1		
Date	Tuesday, December 01, 2020	Sheet	14 of 104

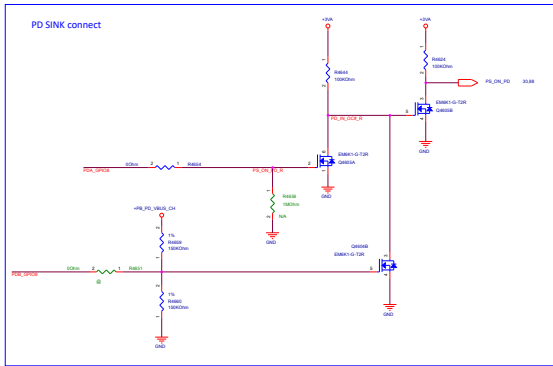




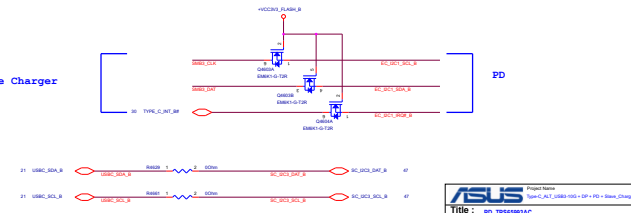
Power Flow Chart



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EC &amp; Slave Charger



<Variant Name>

Title

<Title>

Size

A

Document Number

G512LI

Rev

R1.0

Date:

Tuesday, December 01, 2020

Sheet

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of

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<Variant Name>

Title

<Title>

Size

A

Document Number

G512LI

Rev

R1.0

Date:

Tuesday, December 01, 2020

Sheet

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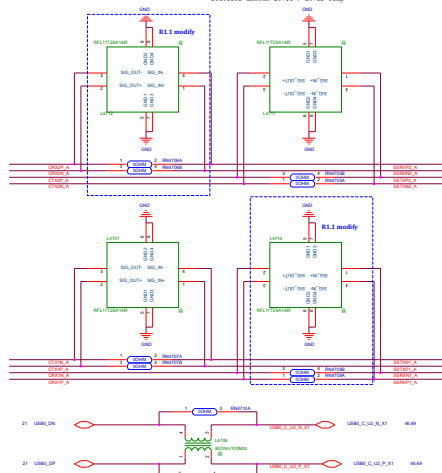
of

104

## USB3.0 EMI

SEMPASS Copyright 2016  
SEMPASS 註冊商標 nba\_fllaw\_gp\_0016  
SEMPASS 註冊商標 nba\_fllaw\_gp\_0016

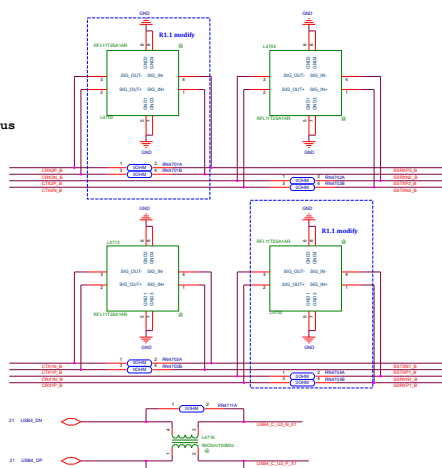
20191202 ashton L4711 / L4712 rev0



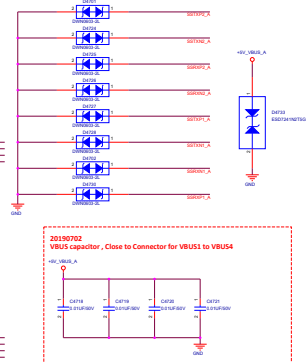
## USB3.0 EMI

SEMPASS Copyright 2016  
SEMPASS 註冊商標 nba\_fllaw\_gp\_0016  
SEMPASS 註冊商標 nba\_fllaw\_gp\_0016

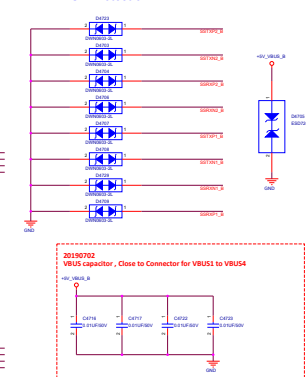
### USB3.0 Bus



## USB3.0 ESD-Protection



## USB3.0 ESD-Protection



NOTE 4 PIN ASSIGNMENT (FRONT VIEW)

Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

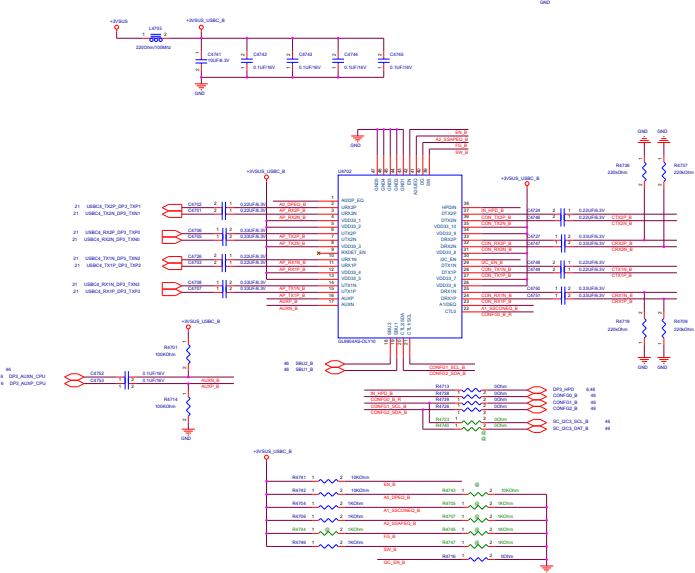
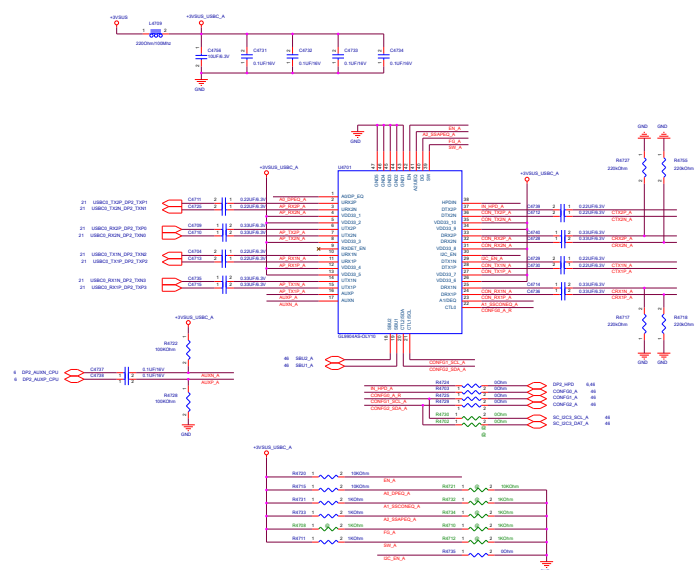
NOTE 4 LATER WELD POINTS MAY BE DISCLOSED.

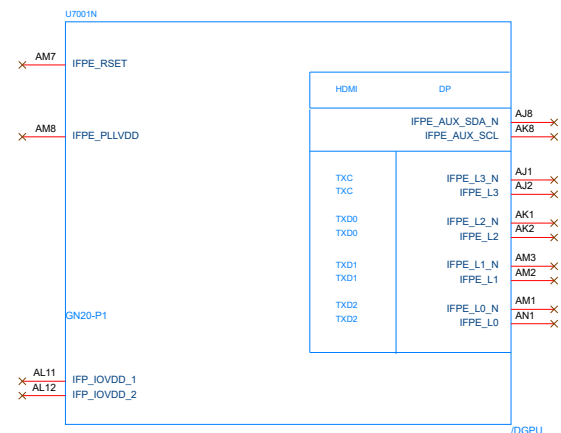
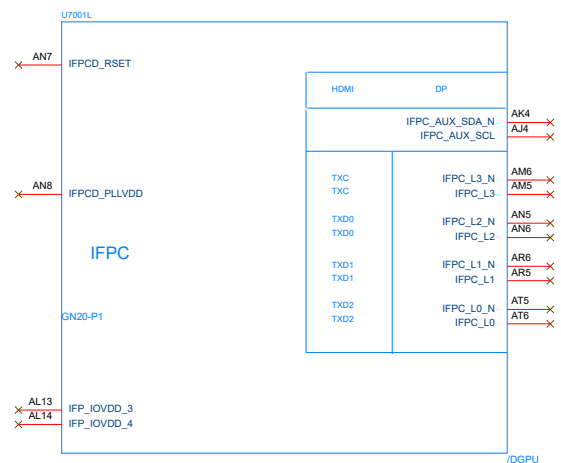
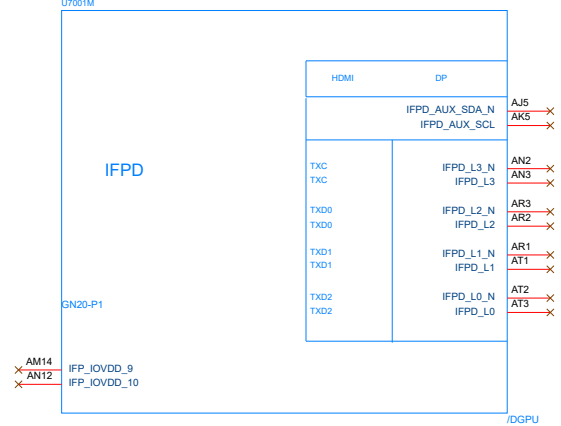
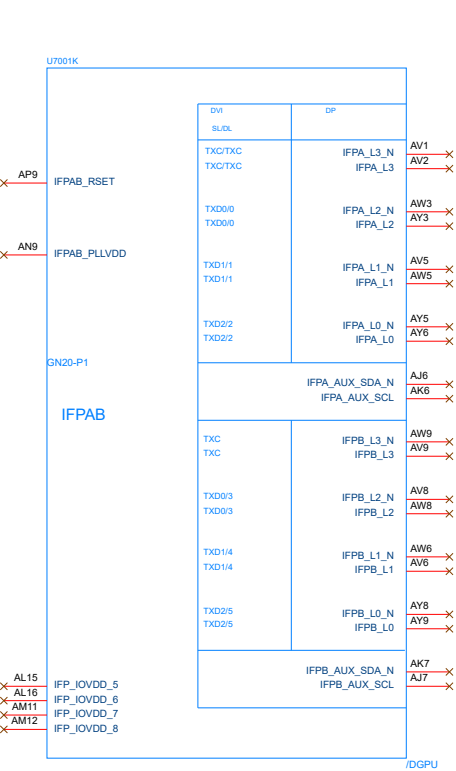



### TYPE-C Connector

### TYPE-C Connector

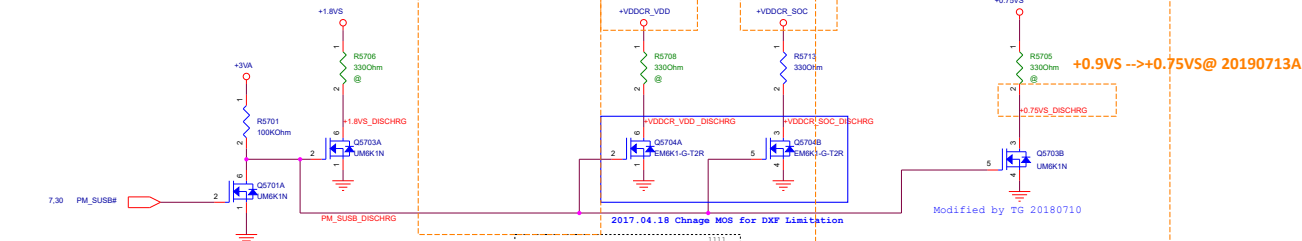
20200410 ashton P130PW12078 (06113-00310100) and GL9904-DLV10 (06113-00570000), Pin to Pin



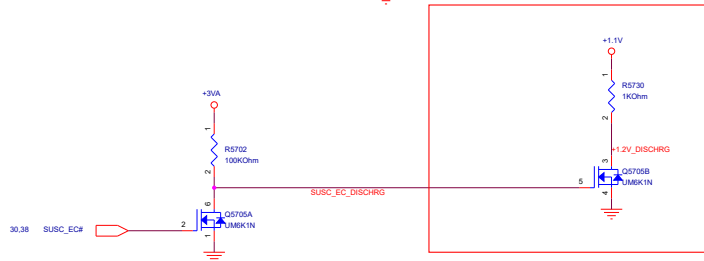
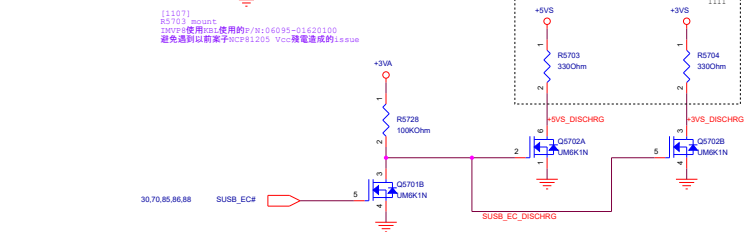


		Project Name		Rev
		<b>Mothereship</b>		R1.1
<b>Title :</b> <b>5G_SUB</b>				
Size  A	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>NR EE RD3</b>			
Date: <b>Tuesday, December 01, 2020</b>			Sheet	<b>55</b> of <b>104</b>

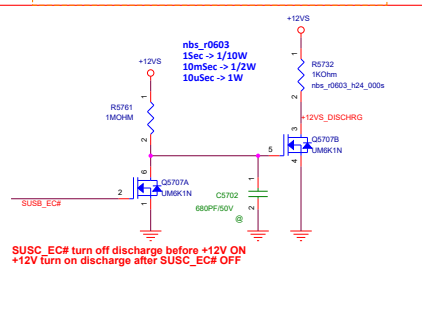
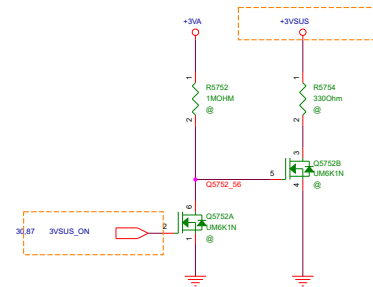




[1107]  
R5703 mount  
20Vpp使用VBI使用的p/n:06095-01620100  
避免遇到以前案子susc#81205 Vcc-發電造成的Issue



R1.1-13

Change DSW to SUS  
@20181009

&lt;Core Design&gt;

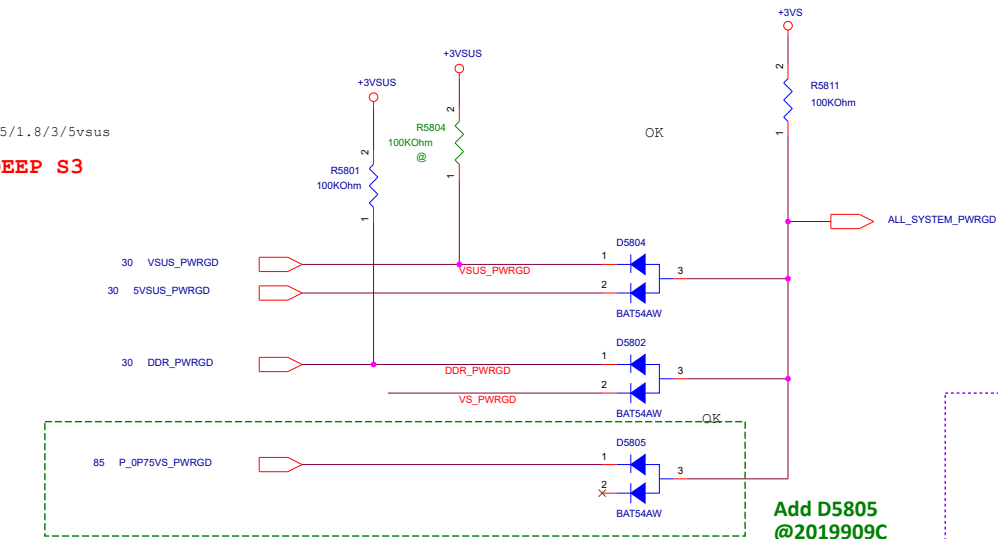
<b>ASUS</b>		Title : DSG_Discharge	
ASUSTek COMPUTER		Engineer: NR EE RD3	
Size Custom	Project Name GX502GX	Rev 1.0	
Date: Tuesday, December 01, 2020	Sheet 57 of 104		



# POWER GOOD DETECTOR

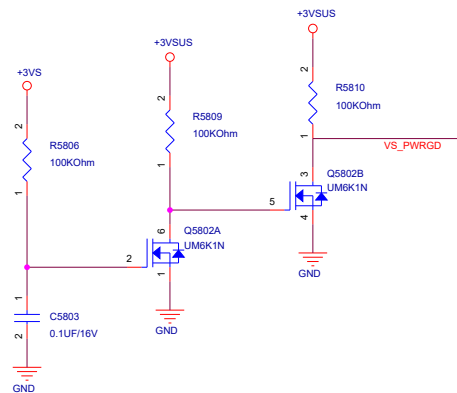
0.95/1.8/3/5vsus

DEEP S3

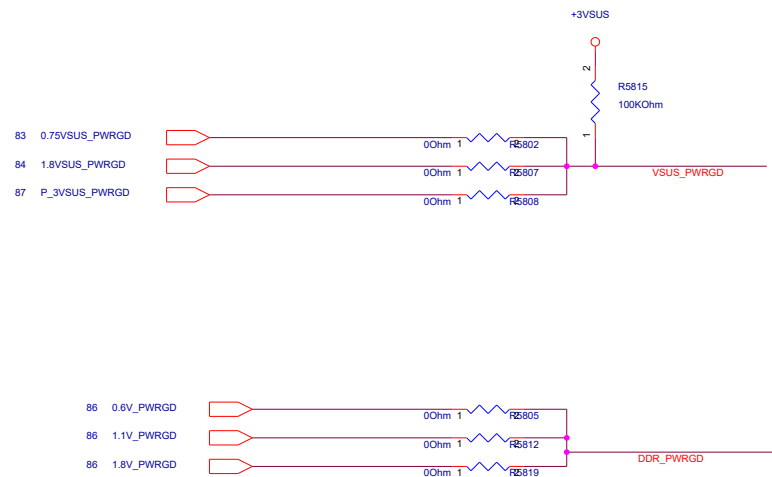


Add D5805  
@2019909C

Power Good



Power Good





**Title :** OTH\_EMI

ASUSTeK COMPUTER

**Engineer:** NR EE RD3

Size

Project Name

Rev

A

**GX502GX**

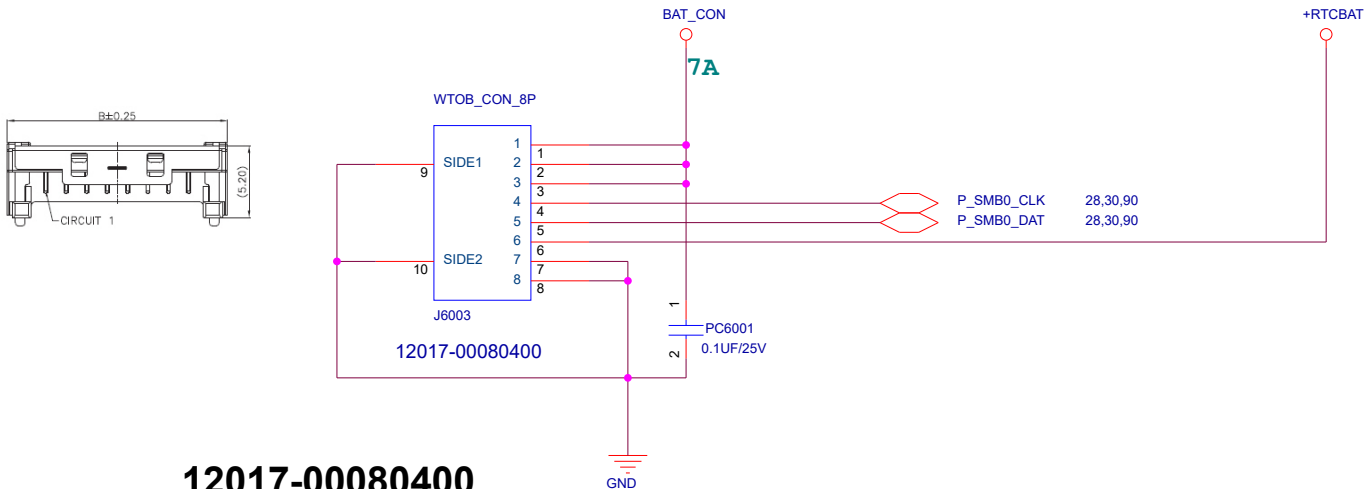
1.0

Date: Tuesday, December 01, 2020

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Battery Connector


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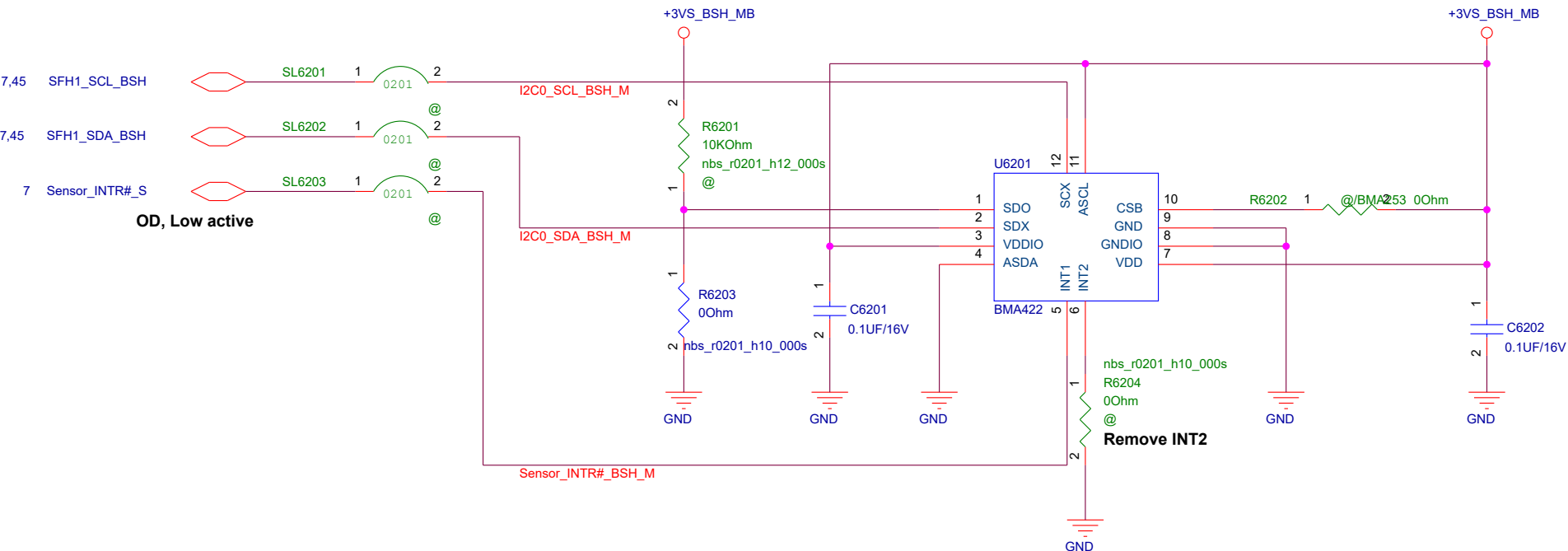
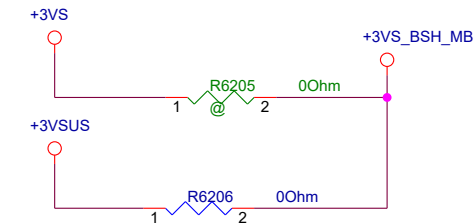
12017-00080400


Note: Battery Connector 正確性與BAT1\_IN\_OC#是否預留!

		Project Name			Rev	
		GA502IV			R1.0	
Title : DC & BAT IN						
Size		Dept.:		Engineer:		
A4		NB_Power team		NR EE RD3		
Date: Tuesday, December 01, 2020				Sheet	60	of 104


		<b>Title :</b> BT_Bluetooth	
ASUSTeK COMPUTER		<b>Engineer:</b> NR EE RD3	
Size  A	Project Name  <b>GX502GX</b>		Rev  1.0
Date: Tuesday, December 01, 2020		Sheet 61 of 104	

	mount	KXTJ2	BMA255
Pull High	R6201	0001111x (OFh)	0011001x (19h)
Pull Low	R6203	0001110x (OEh) (Default)	0011000x (18h) (Default)



		<b>Title :</b> BSH_Sensor
<b>ASUSTeK COMPUTER</b>		<b>Engineer:</b> NR EE RD3
Size  A	Project Name  GL752VW	Rev  1.0

<Variant Name>

		<b>Title :</b> <b>NGFF SSD(MAXIM)</b>	
<b>ASUSTeK COMPUTER</b>		<b>Engineer:</b> <b>NR EE RD3</b>	
Size	Project Name		Rev
D	<b>GL752VW</b>		1.0
Date: <b>Tuesday, December 01, 2020</b>		Sheet <b>63</b> of <b>104</b>	



<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

Date:

Tuesday, December 01, 2020

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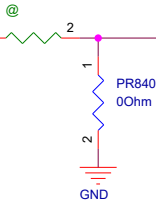
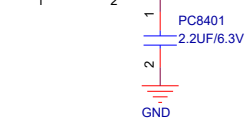
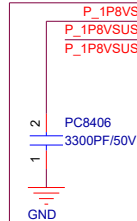
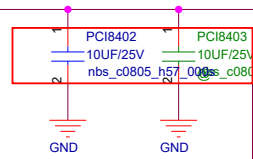
# +1.8VSUS [For PCH]

AC\_BAT\_SYS

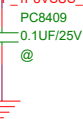
+5VSUS

+5VSUS

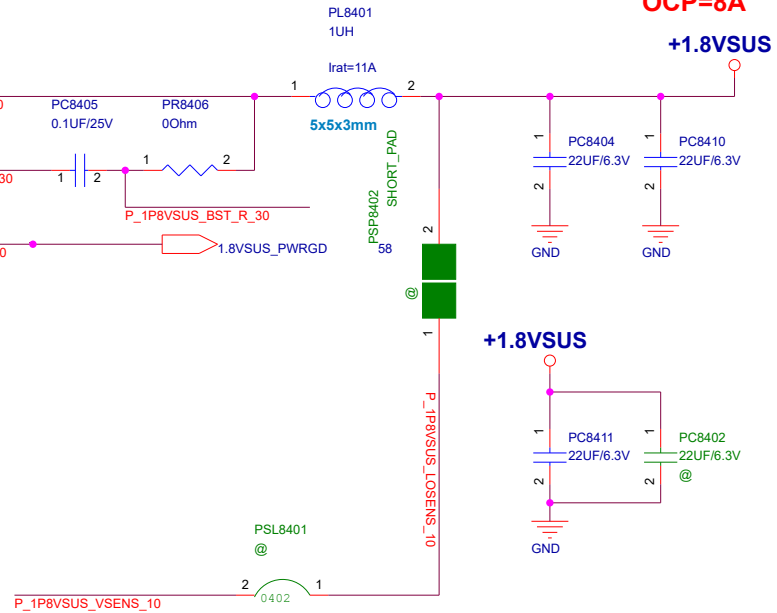
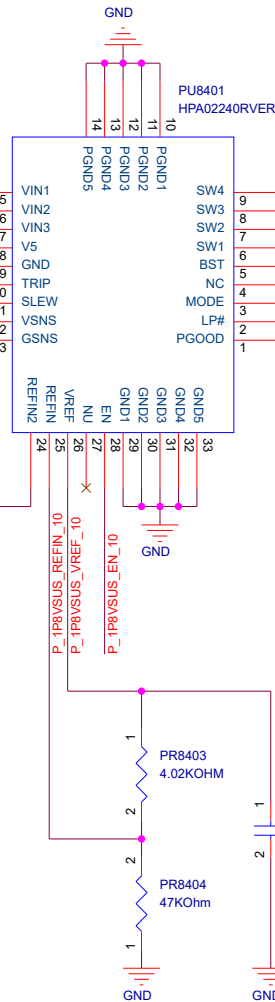
30 1.8VSUS\_ON



PR8407  
00hm

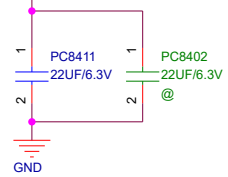


PT840\* 請放置 PU8401旁;並請放置Trace 上!



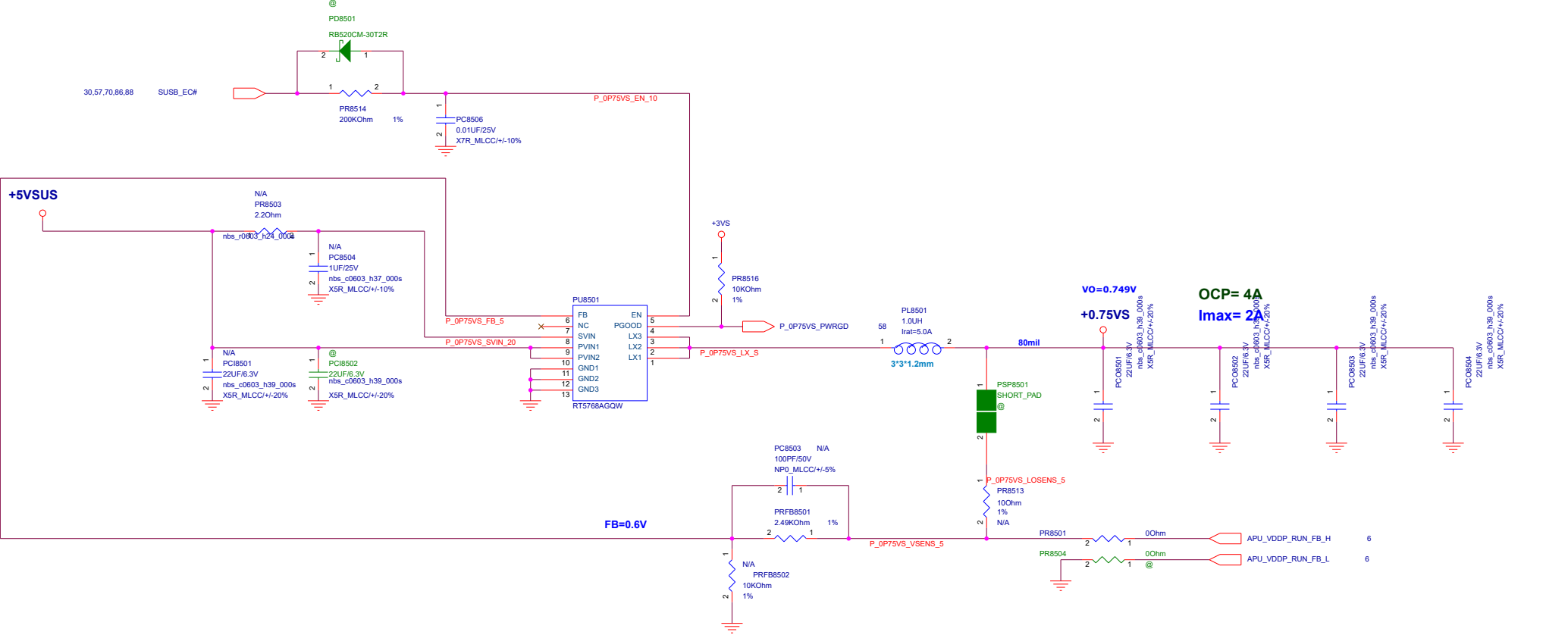
I<sub>max</sub> = 3.5A  
OCP=8A  
+1.8VSUS

+1.8VSUS



<Variant Name>

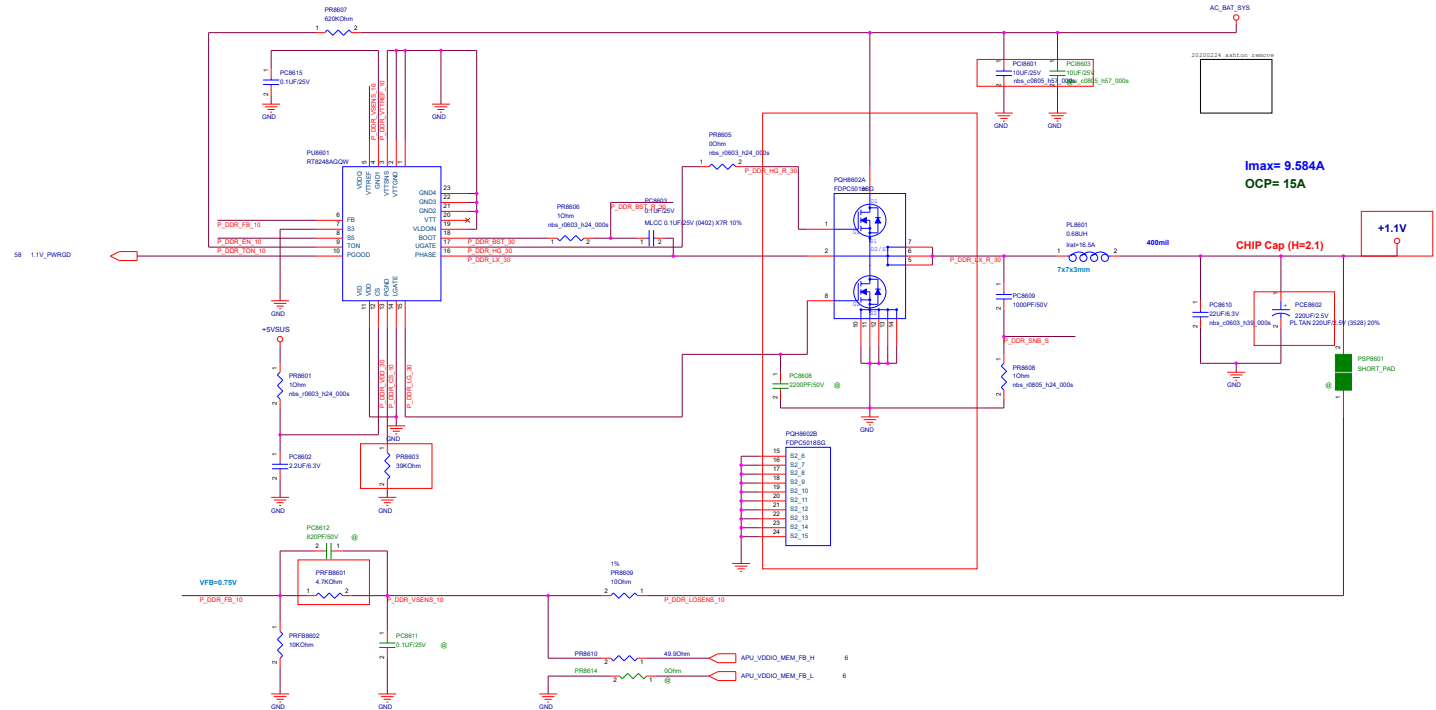
Project Name		Rev
ASUS Project Name		R1.0
Title : PW_+1.8VSUS		
Size A4	Dept.: NB Power team	Engineer: NR EE RD3
Date: Tuesday, December 01, 2020	Sheet 84	of 104



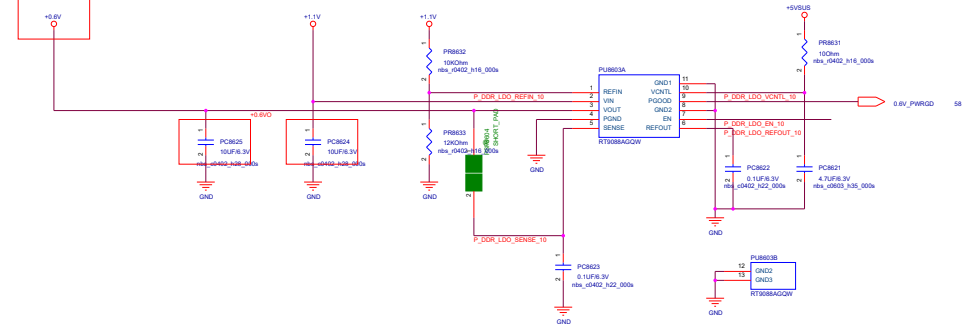
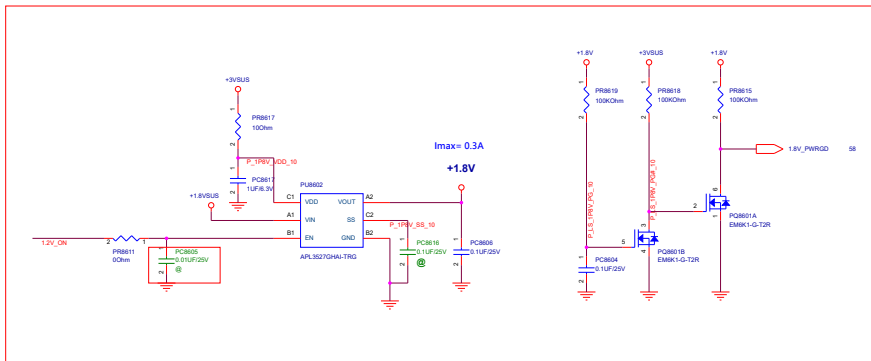
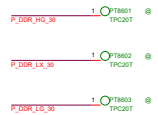
<Variant Name>

Project Name		Rev
ASUS GA503QS		R1.0
Title : PW_+0.75VS		
Size	Dept.: NB Power team	Engineer: CS Lin
A3	Date: Tuesday, December 01, 2020	Sheet 85 of 104

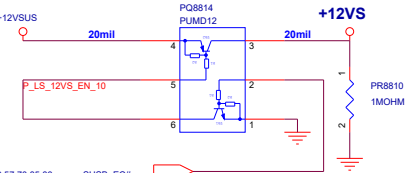
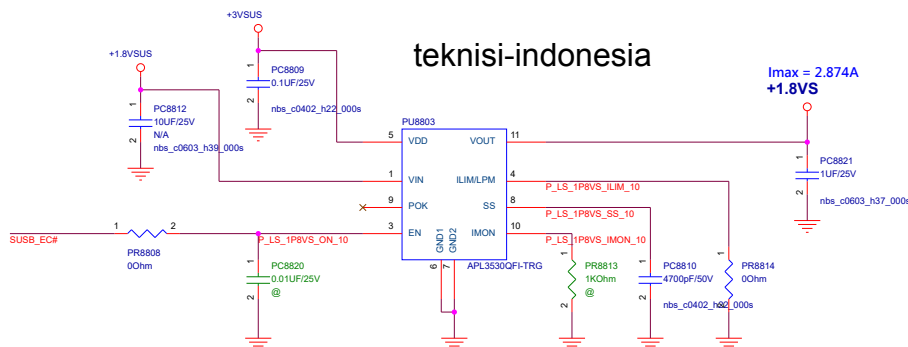
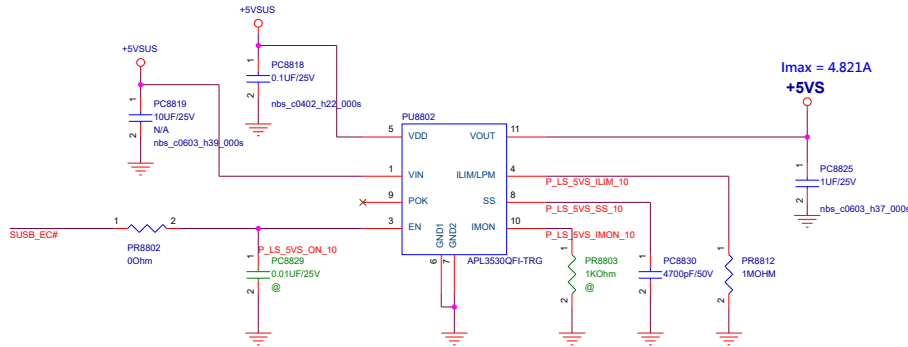
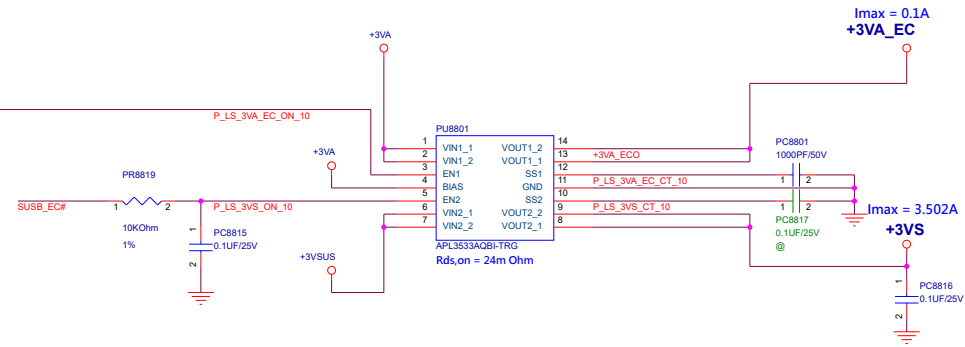
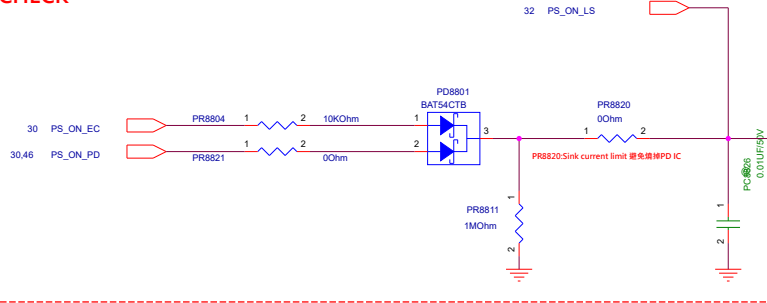
**+1.1V / +VTT / +2.5V[For Memory]**



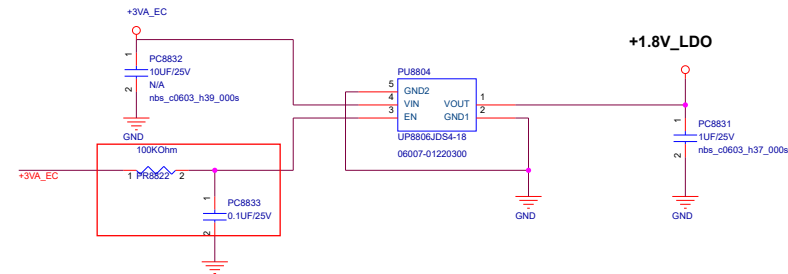
PT860\* 請放置 PU8600旁;並請放置Trace 上!



# EE CHECK



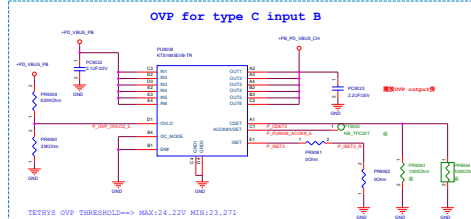
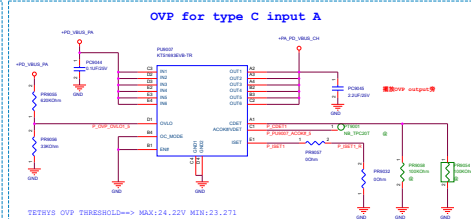
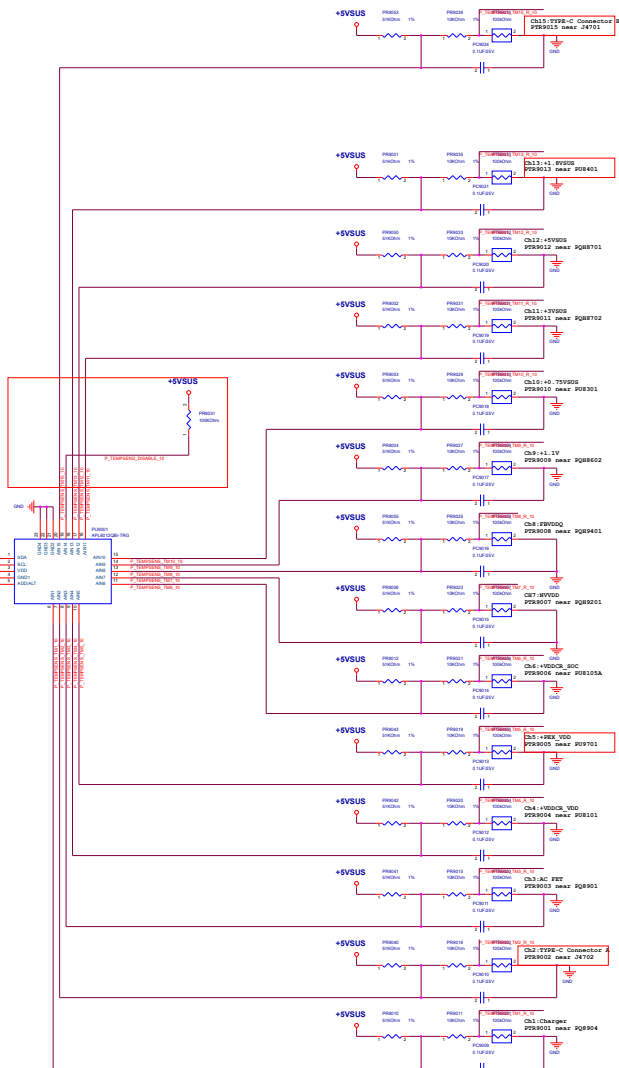
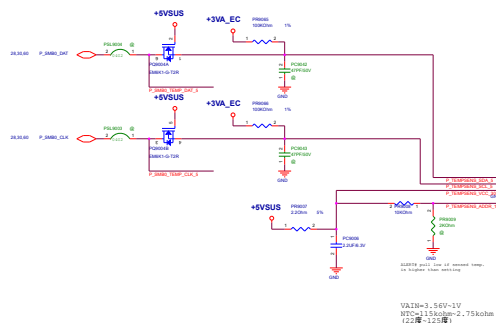
## +1.8V\_LDO Power For EC SPI ROM

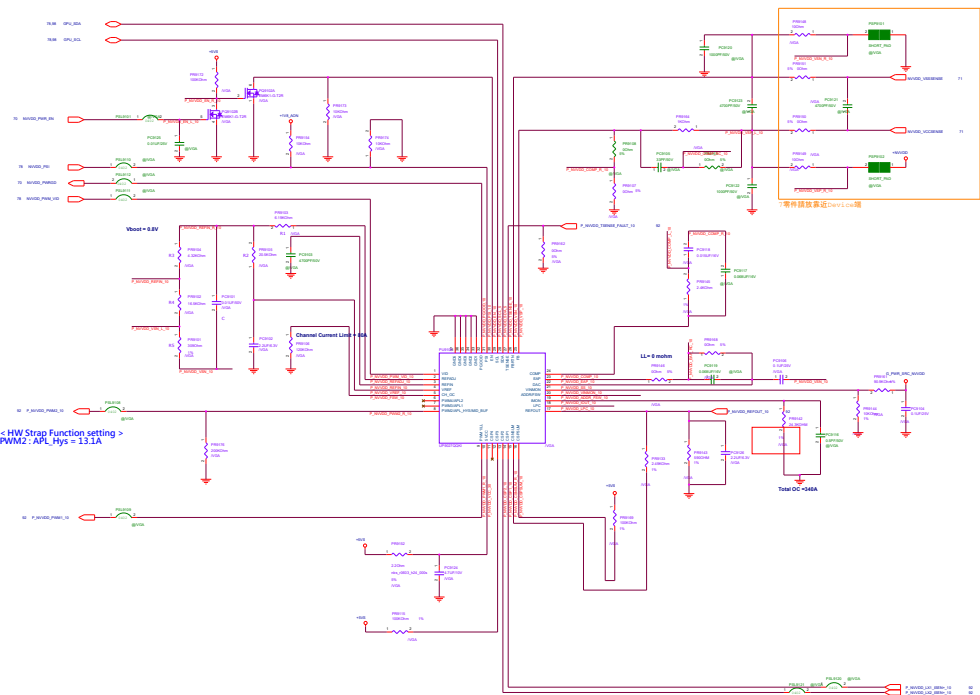


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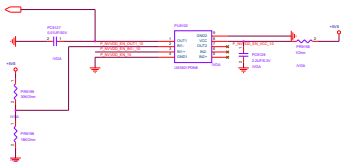
Address	Ca10	Ca11	Ca12	Ca13	Ca14	Ca15	Ca16	Ca17
000001	10a	1-10a	0a	1-10a	1-10a	1-10a	1-10a	0a
000002	0	0	0-0a	0-0a	0-0a	0-0a	0-0a	0

Register Address							
Address	DaD0	DaD1	DaD2	DaD3	DaD4	DaD5	DaD6
0x0	0	0	0	0	0	0	0
Power-On	Temp. alert threshold setting			Demand temp. data			bit 6 = 1 bit 5 = 0 bit 4 = 1  When SLEWDS is active



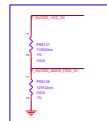
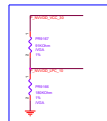


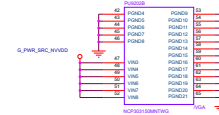
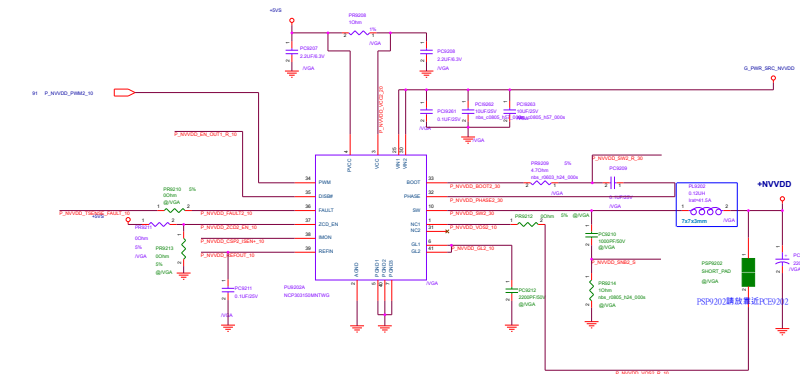
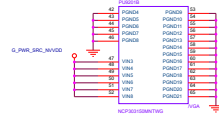
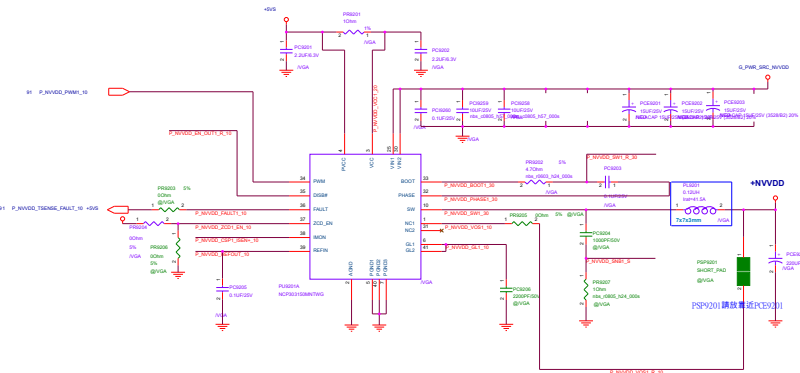
© 2000 Blackwell Science Ltd



```
Low Phase Count( LPC )
* Cold Boot : 2 Phase
Warm Boot : 1 Phase
```

```
Address / Fsw
* Fsw = 400kHz( Discrete )
* Address : 0x40
```







<Variant Name>

Title

<Title>

Size

A4

Document Number

<Doc>

Rev

<RevCode>

Date:

Tuesday, December 01, 2020

Sheet

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of

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+FBVDDQ [For VRAM]

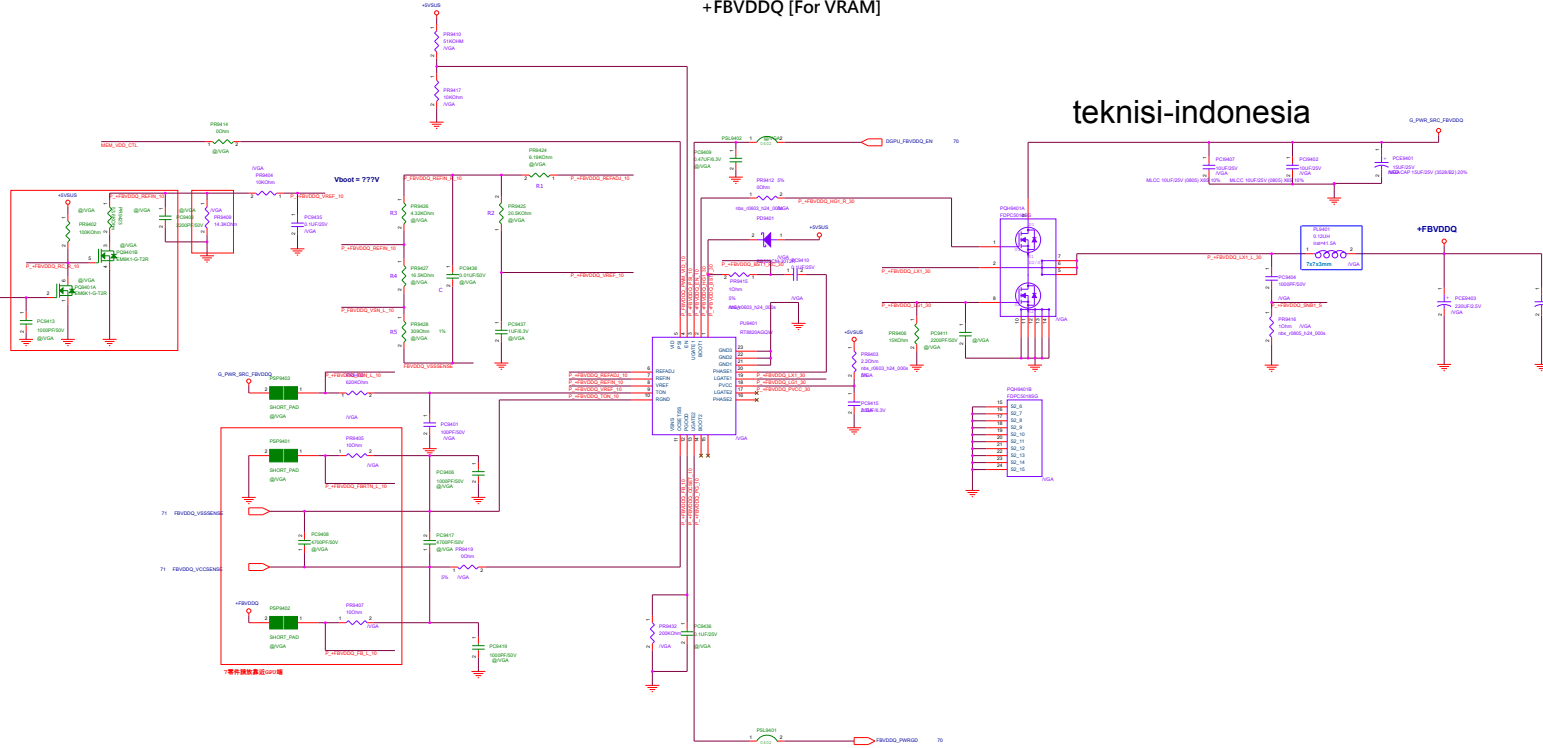
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DVS Setting			
MDM_VDD_CTL	#		L
Voltage	1.35V		1.35V
993404		15000ns	
993409		21.0000ns	
993423		75000ns	

DVS Setting			
MDM_VDD_CTL	#		L
Voltage	1.35V		1.35V
993404		15000ns	
993409		21.0000ns	
993423		57.0000ns	

DVS Setting			
MDM_VDD_CTL	#		L
Voltage	1.35V		1.35V
993404		15000ns	
993409		14.0000ns	
993423		140000ns	

Fixed Vout			
#	IC#403/PB403/PB403	IC#403/PB403	
Voltage	1.35V		1.35V
993404		15000ns	
993409		14.0000ns	



PT9401 諸設置 P9402 諸設置 Trace 2.1

P9401  
 P9402  
 P9403  
 P9404



Project Name

2021Forever

Rev

R1.0

**Title :** Choke\_PCB\_Footprint

Size

A

**Dept.:** NB Power Team

**Engineer:** Power

Date: Tuesday, December 01, 2020

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Project Name

2021Forever

Rev

R1.0

**Title :** Choke\_PCB\_Footprint

Size

A

**Dept.:** NB Power Team

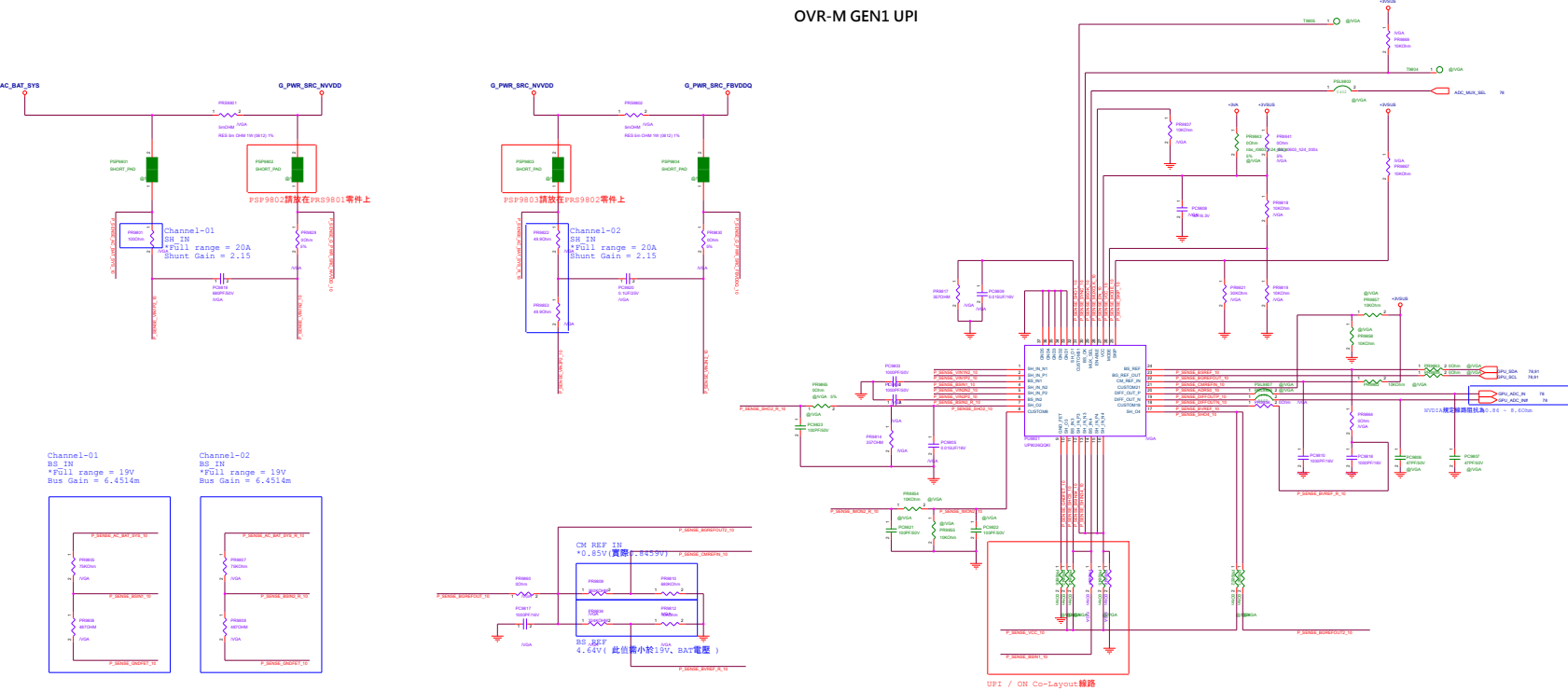
**Engineer:** Power

Date: Tuesday, December 01, 2020

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# OVR-M GEN1 UPI



	PR9801	PR9805	PR9807	PC9803	PC9804	PC9805	PR9814	PR9855	PR9822
GN20	MC9454853MRTWG 06129-00220000	0 Ohm 10G212000004030	0 Ohm 10G212000004030	⌀	⌀	⌀	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
N18P-G1	UP9026GQKT 06129-00110100	75KOhm 10G212750214010	75KOhm 10G212750214010	1000PF/50V 11G232110214321	1000PF/50V 11G232110214321	0.015UF/16V 11G232115311360	3570Ohm 10G212357014010	⌀	49.90Ohm 10G212498914010

	PC9810	PR9860	PR9809	PR9810	PR9834	PR9863	PR9859	PC9809	PR9808
GN20	⌀	⌀	⌀	10KOhm 10G212100214010	31.6KOhm 10G212316214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	⌀	⌀
N18P-G1	1000PF/16V 11G232110211030	0 Ohm 10G212000004030	360KOhm 10G212364004010	680KOhm 10G212680314010	324KOhm 10G212324314010	⌀	⌀	0.015UF/16V 11G232115311360	4870Ohm 10G212487014010

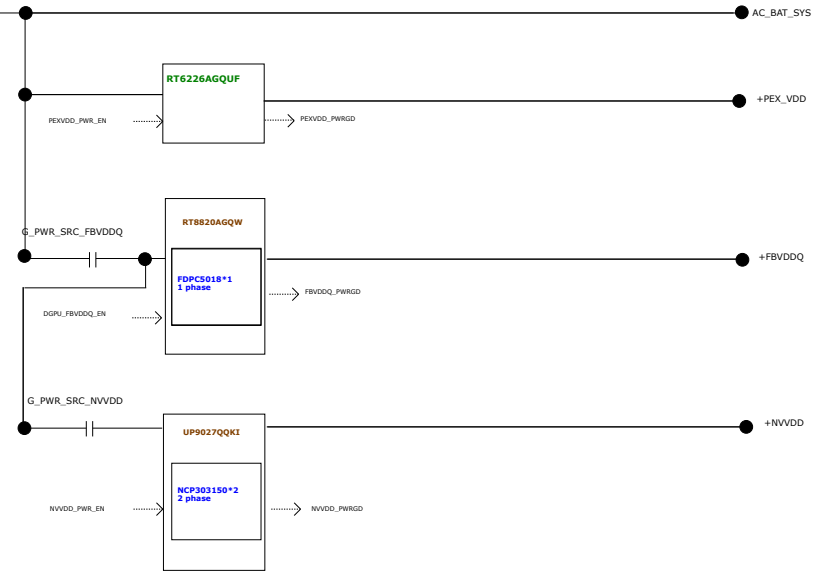
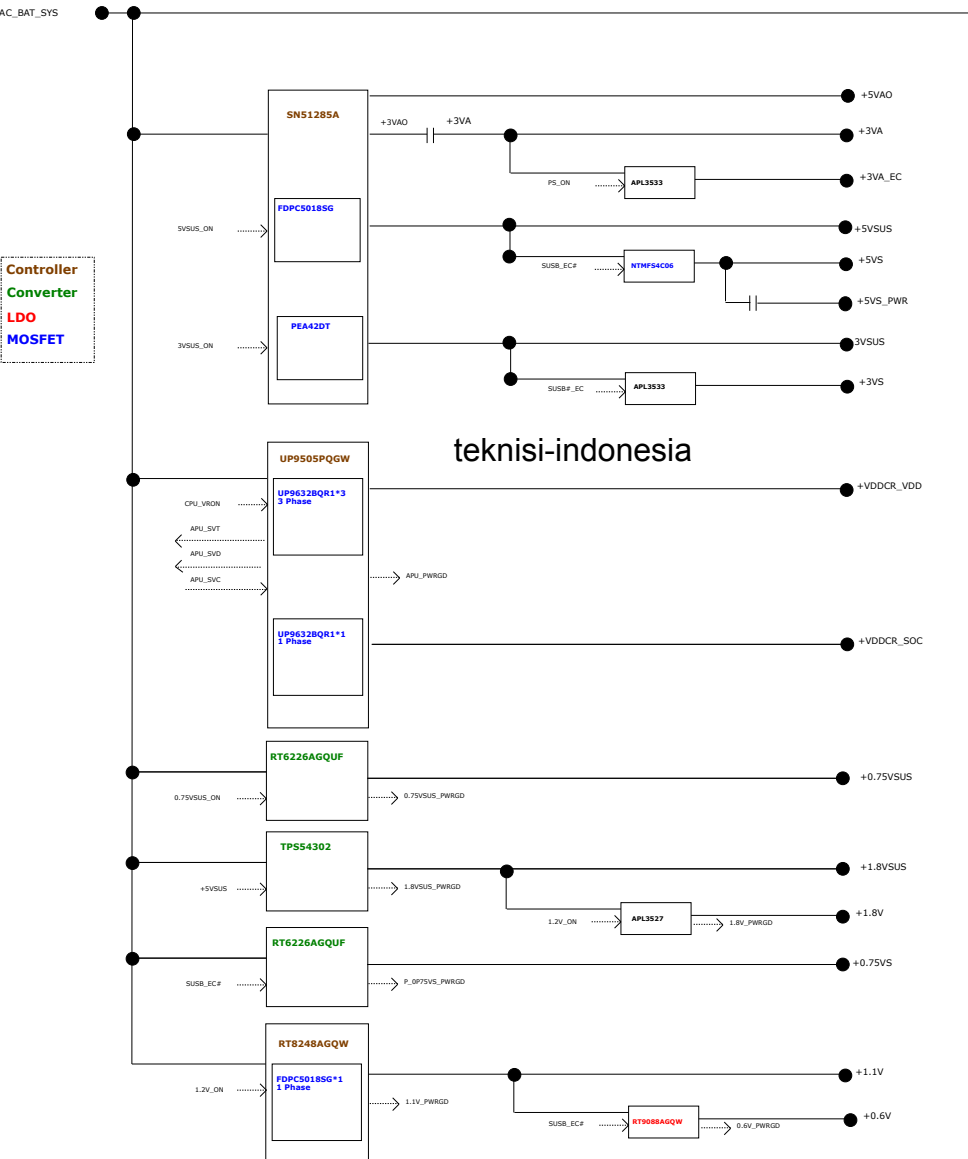
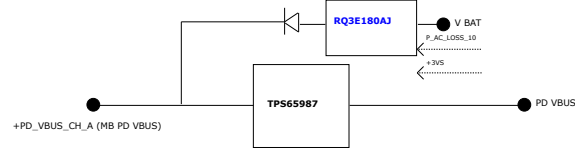
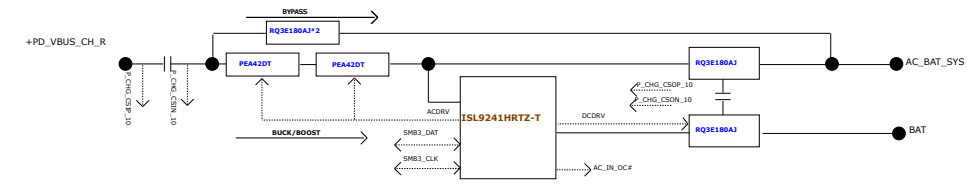
  

	PR9806	PR9861	PR9864	PR9857	PR9801	PR9853	PR9817	PR9844/PR9845	PR9846/PR9847
GN20	⌀	0 Ohm 10G212000004030	⌀	10KOhm 10G212100214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	⌀	0 Ohm 10G212000004030	⌀
N18P-G1	4870Ohm 10G212487014010	⌀	0Ohm 10G212000004030	⌀	1000Ohm 10G212100014010	49.90Ohm 10G212498914010	3570Ohm 10G212357014010	⌀	0 Ohm 10G212000004030

	PR9866	PR9818/PR9819	PR9821
GN20	0 Ohm 10G212000004030	⌀	⌀
N18P-G1	⌀	10KOhm 10G212100214030	30KOhm 10G212300214010

Customer Name

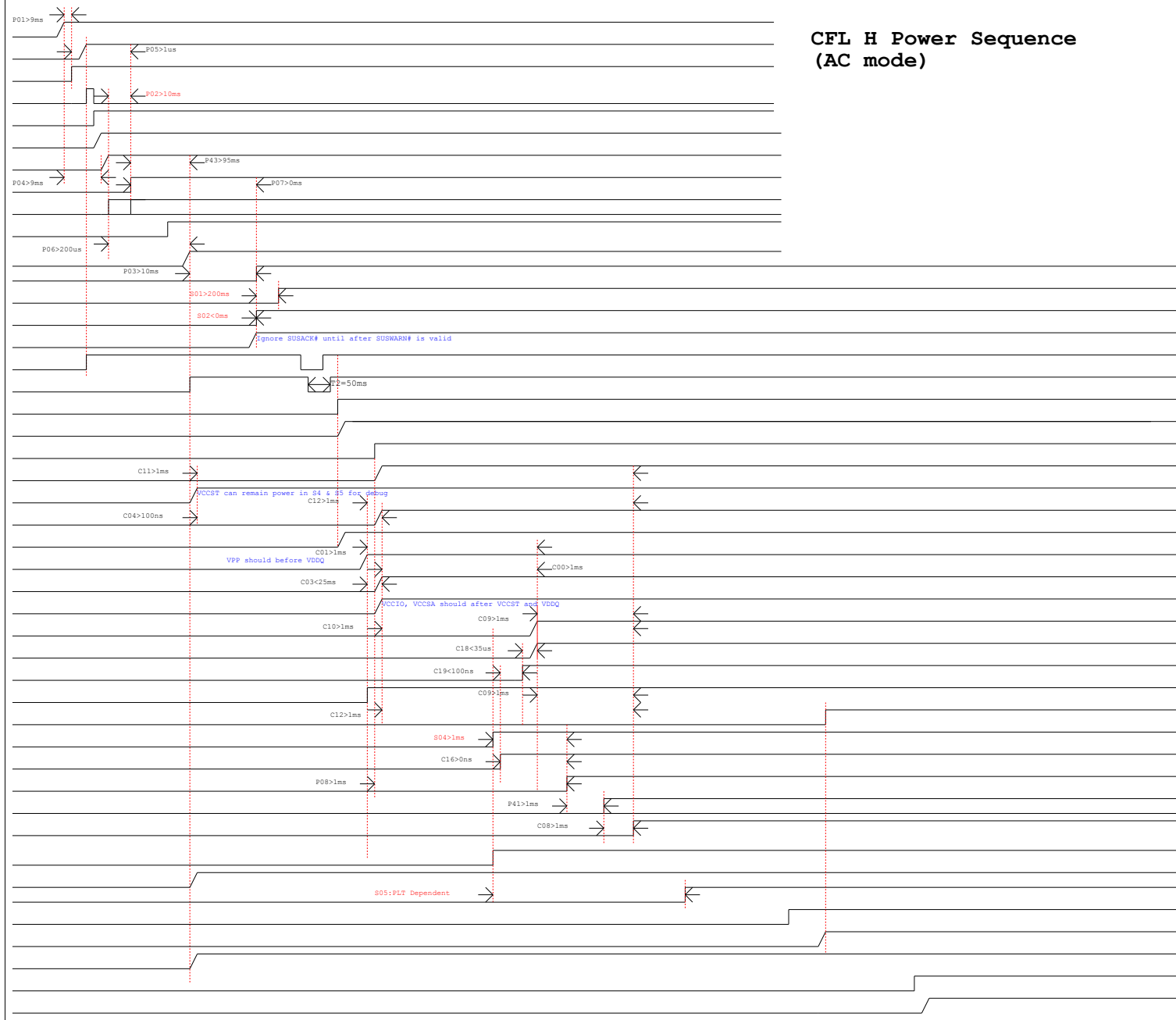


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C:CPU  
P:PCH  
S:PLT  
Power  
Signal

(+RTCBAT)+3VA\_RTC  
(AC\_BAT\_SYS)+3VA/+5VA  
(+3VA\_RTC)RTCRST#(PCH)  
(Power)AC\_IN\_OC#(EC)  
(EC)PS\_ON(+3VA\_EC)  
(PS\_ON)+3VA\_EC(EC)  
(3VADSW\_ON)+3VA\_DSW(3VA\_DSW\_PWRGD)  
(EC)DPWROK\_EC(PCH)  
(+3VA\_DSW)PM\_BATLOW#(PCH)  
(PCH)PM\_SLP\_SUS#(EC)  
(VSUS\_ON)+1.0VSUS\_VCCPRIM(1.0VSUS\_PWRGD)  
(EC)PM\_RSMRST#\_PCH(PCH)  
(PCH)SUSWARN#(EC)  
(EC)ME\_AC\_PRESENT\_PCH(PCH)  
(EC)PCH\_SUSACK#(PCH)  
(PWR\_Switch)PWR\_SW#(EC)  
(EC)PM\_PWRBTN#(PCH)  
(EC)SUSC\_EC#(Power)  
(SUSC\_EC#)+12V/+5V/+3V  
(EC)SUSB\_EC#(Power)  
(SUSB\_EC#)+12VS/+5VS/+3VS  
(SUSB\_EC#)+1.0V\_VCCST,VCCPLL  
(SUSB\_EC#)+VCCIO,(+12VS)+VCCSTG  
(1.2V\_ON)+2.5V(2.5V\_PWRGD)  
(1.2V\_ON)+VDDQ\_CPU(1.2V\_PWRGD)  
(+12VS)+VCCPLL\_OC  
(SUSB\_EC#)+VCCIO(VCCIO\_PWRGD)  
(ALL\_SYSTEM\_PWRGD)+VCCSA(IMVP8\_PWRGD)  
(DDR\_VTT\_CTRL)+0.6V  
(CPU)DDR\_VTT\_CTRL(Power)  
(Power)1.2V\_PWRGD(AND)  
(Power)IMVP8\_PWRGD  
(AND)ALL\_SYSTEM\_PWRGD(CPU/PCH/EC/Power)  
(ALL\_SYSTEM\_PWRGD)VCCST\_PWRGD\_CPU(CPU)  
(EC)PM\_PWROK\_PCH(PCH)  
(PCH)CLK\_PCH\_BCLK(CPU)  
(PCH)H\_CPUPWRGD(CPU)  
  
(CPU)P\_SVID\_DATA\_X2(Power)  
(EC)PM\_SYSPWROK\_PCH(PCH)  
(PCH)PLT\_RST#(CPU/EC/Device)  
(P\_IMVP8\_DRVON)+VCCCORE(IMVP8\_PWRGD)  
(CPU)H\_THERMTRIP#(PCH)  
(PCH)DDR4\_DRAMRST#(Memory)

+VCCGT

CFL H Power Sequence  
(AC mode)

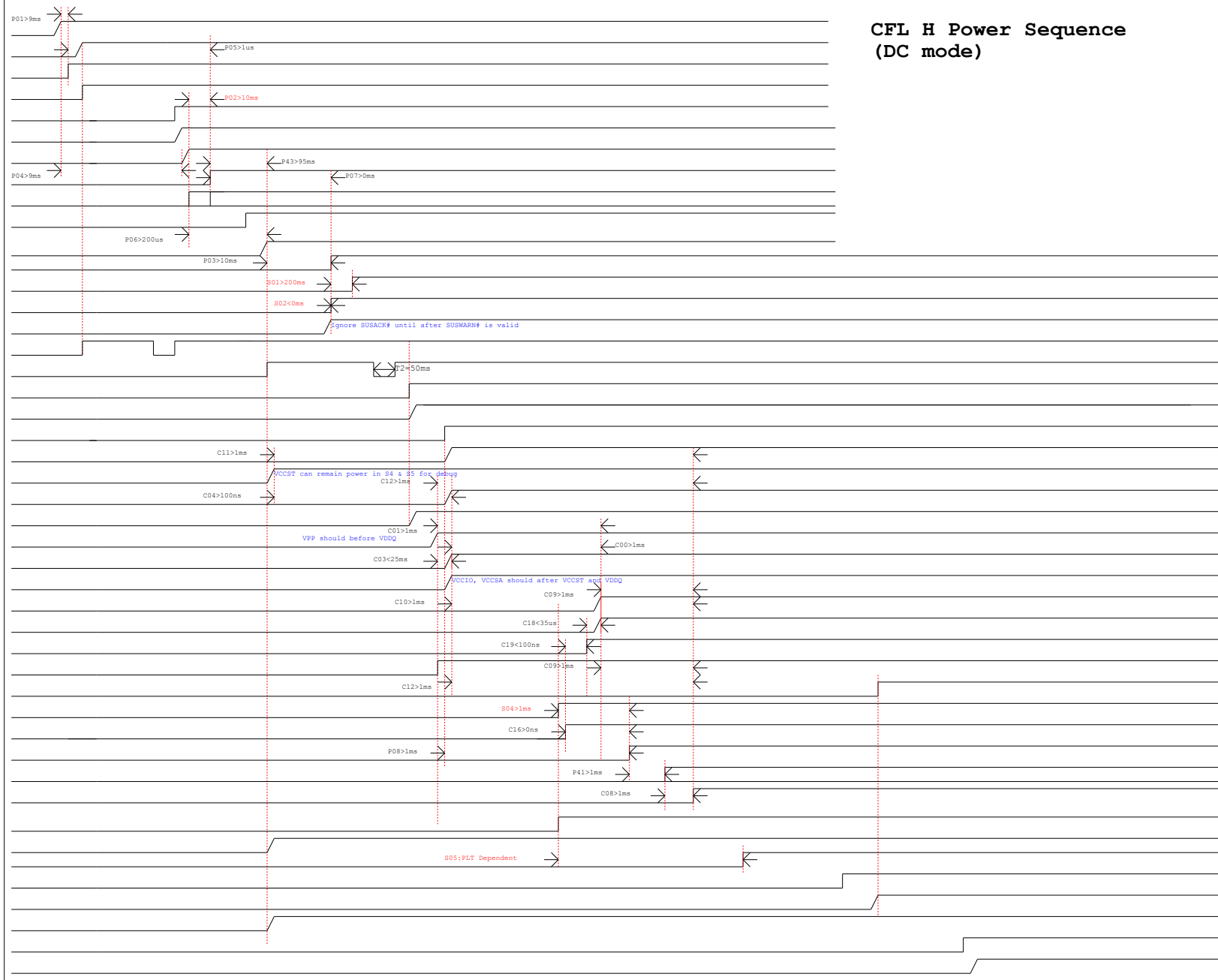


# DC-IN Mode

C:CPU (+RTCBAT)+3VA\_RTC  
 P:PCH (AC\_BAT\_SYS)+3VA/+5VA  
 S:PLT (+3VA\_RTC)RTCST#(PCH)  
 Power (Power)AC\_IN\_OC#(EC)  
 Signal (EC)PS\_ON(+3VA\_EC)  
 (PS\_ON)+3VA\_EC(EC)  
 (3VADSW\_ON)+3VA\_DSW(3VA\_DSW\_PWRGD)  
 (EC)DPWROK\_EC(PCH)  
 (+3VA\_DSW)PM\_BATLOW#(PCH)  
 (PCH)PM\_SLP\_SUS#(EC)  
 (VSUS\_ON)+1.0VSUS\_VCCPRIM(1.0VSUS\_PWRGD)  
 (EC)PM\_RSMRST#\_PCH(PCH)  
 (PCH)SUSWARN#(EC)  
 (EC)ME\_AC\_PRESENT\_PCH(PCH)  
 (EC)PCH\_SUSACK#(PCH)  
 (PWR\_Switch)PWR\_SW#(EC)  
 (EC)PM\_PWRBTN#(PCH)  
 (EC)SUSC\_EC#(Power)  
 (SUSC\_EC#)+12V/+5V/+3V  
 (EC)SUSB\_EC#(Power)  
 (SUSB\_EC#)+12VS/+5VS/+3VS  
 (VSUS\_ON)+1.0V\_VCCST,VCCPLL(VCCST\_PWRGD)  
 (+VCCIO)+VCCSTG  
 (1.2V\_ON)+2.5V(2.5V\_PWRGD)  
 (1.2V\_ON)+VDDQ\_CPU(1.2V\_PWRGD)  
 (+12VS)+VCCPLL\_OC  
 (SUSB\_EC#)+VCCIO(VCCIO\_PWRGD)  
 (ALL\_SYSTEM\_PWRGD)+VCCSA(IMVP8\_PWRGD)  
 (DDR\_VTT\_CTRL)+0.6V  
 (CPU)DDR\_VTT\_CTRL(Power)  
 (Power)1.2V\_PWRGD(AND)  
 (Power)IMVP8\_PWRGD  
 (AND)ALL\_SYSTEM\_PWRGD(CPU/PCH/EC/Power)  
 (ALL\_SYSTEM\_PWRGD)VCCST\_PWRGD\_CPU(CPU)  
 (EC)PM\_PWROK\_PCH(PCH)  
 (PCH)CLK\_PCH\_BCLK(CPU)  
 (PCH)H\_CPU\_PWRGD(CPU)  
 (ALL\_SYSTEM\_PWRGD)P\_IMVP8\_EN\_10(Power)  
 (CPU)P\_SVID\_DATA\_X2(Power)  
 (EC)PM\_SYSPWROK\_PCH(PCH)  
 (PCH)PLT\_RST#(CPU/EC/Device)  
 (P\_IMVP8\_DRVON)+VCCCORE(IMVP8\_PWRGD)  
 (CPU)H\_THERMTRIP#(PCH)  
 (PCH)DDR4\_DRAMRST#(Memory)

+VCCGT

## CFL H Power Sequence (DC mode)





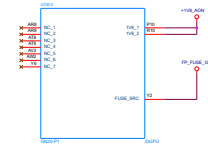
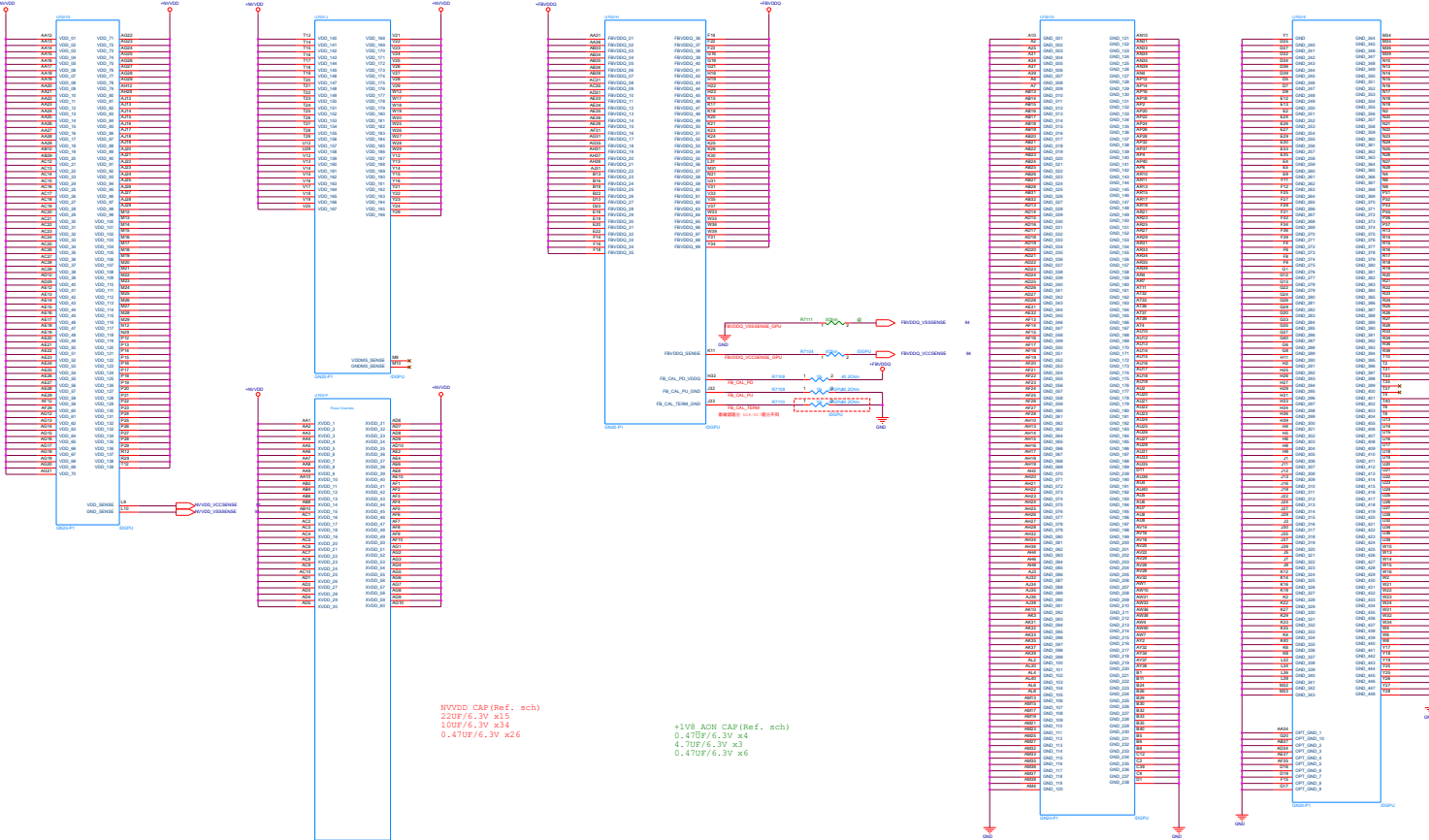
1. P.01-30 reference FA50500, P.11-104 reference GX502\_(WV39\_20180927C)  
2. Ref. connection\_WV79\_20180928a)  
20181004  
P.03  
P.07  
P.30 Copy FX5050DY P.30  
P.32 Modify Reset circuit  
P.34 Modify LAN connector  
P.35 Modify N-KEY I78291E to I78299E  
P.36 修改  
P.37 Modify Headphone\_Mic, ESS  
P.39 Remove Mute control  
P.40 Modify circuit  
P.41 Modify circuit 4 喇叭, 0 ohm电阻  
P.43 Add Mic and HSR circuit  
P.48 Keep SL4802  
P.49 Modify circuit  
P.50

9. Card Reader: AD6435--026630002400 (Page42)

10. USB Charger IC: (Page52) Sillego SLG55584AVTR -- 06016-00040000  
MAXIM MAX14566AESTA+ -- 060016196011

11. USB3.0 Repeater IC: (Page67)  
Parade : P88710B -- 06053-00200000  
Maxim : MAX14972CTG+ -- 06053-00030000

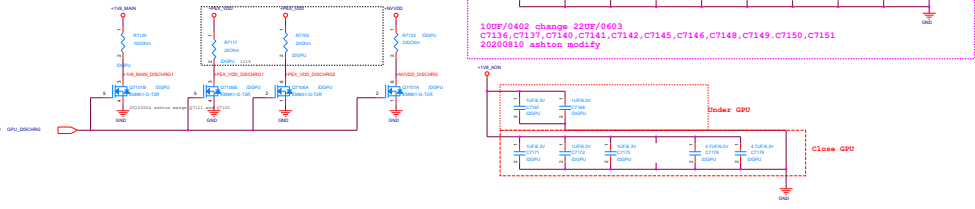
		Title : <a href="#">ASUS MAX Series 2018</a>	
Product Name		Engineer : <a href="#">WITE REE</a>	
Rev	Revision	GX5020X	Rev
01	Rev. 000000000000	000	00



1V8VDD CAP (Ref. sch)  
220P/6.3V x15  
100T/6.3V x34  
0.47UF/6.3V x26

+1V8 AON CAP (Ref. sch)  
0.47UF/6.3V x4  
0.70UF/6.3V x3  
0.47UF/6.3V x6

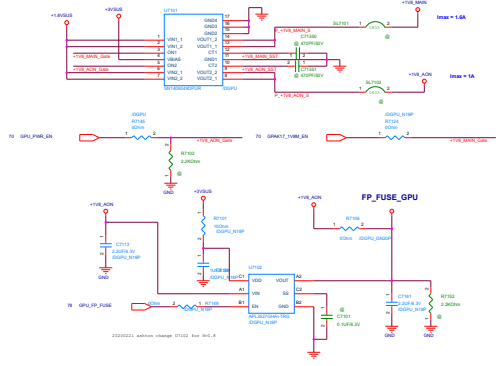
Discharge



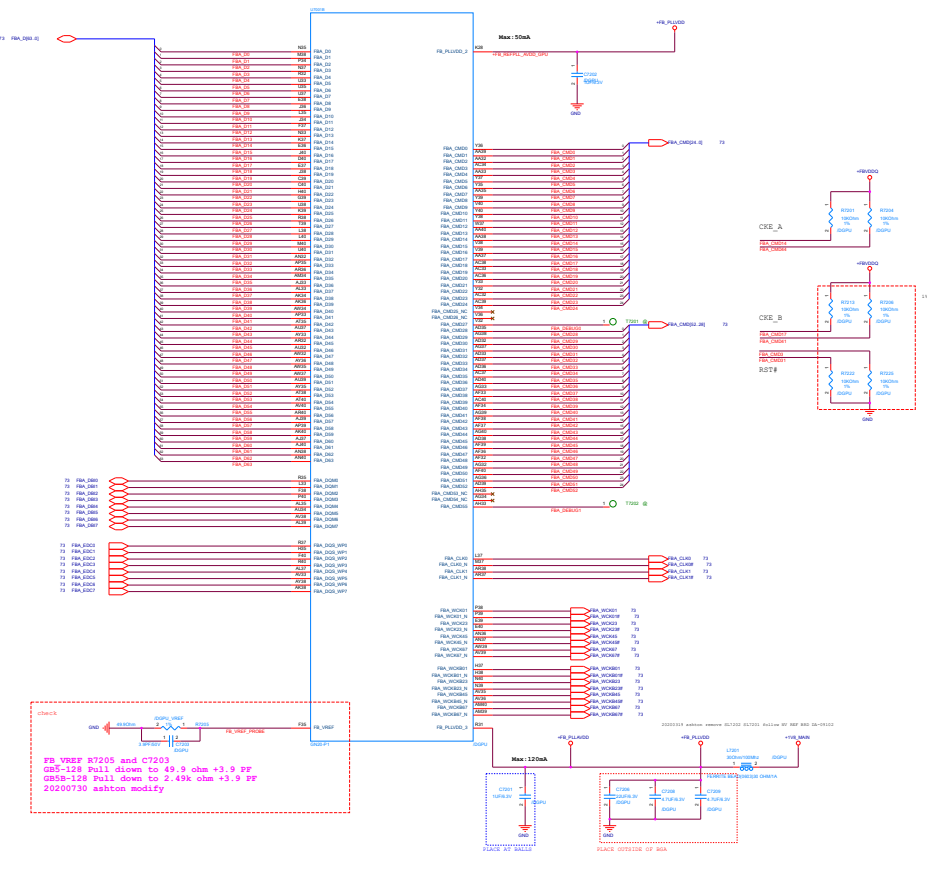
Remove C7160/C7157  
20200810 ashton modify

1V8 Power Control

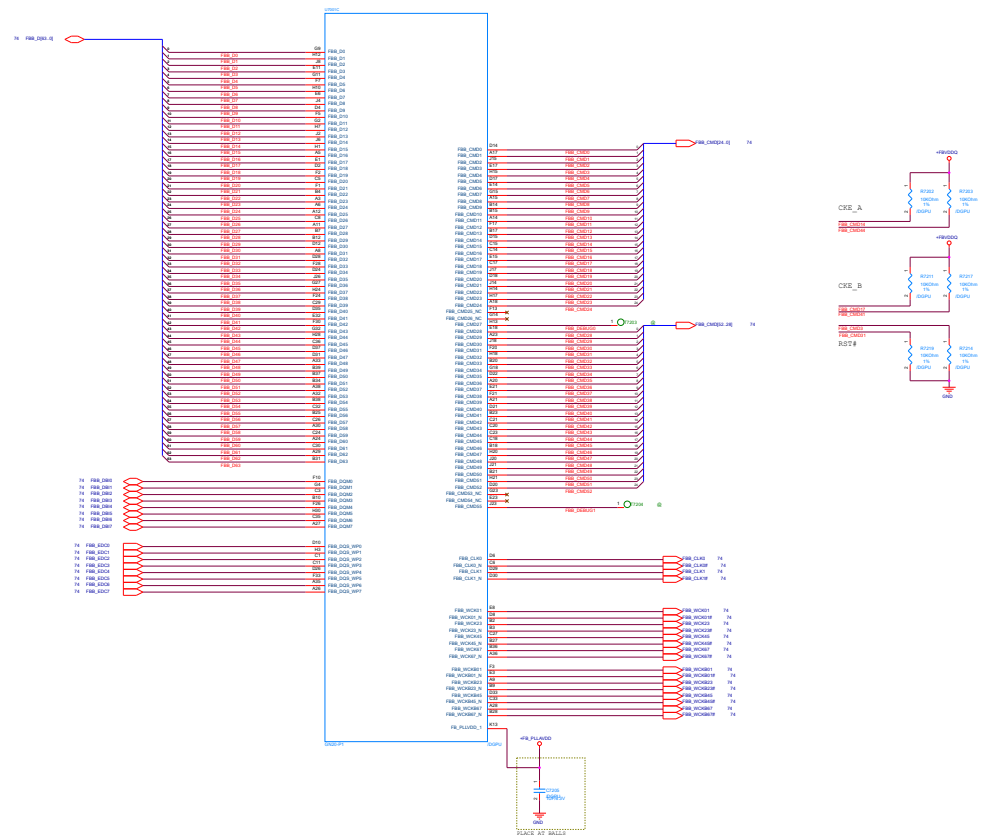
1V8 Power merge RT103  
20200730 ashton modify



**MEMORY: GPU FB Partition A**



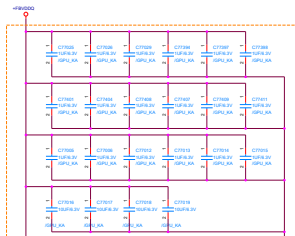
**MEMORY: GPU FB Partition B**



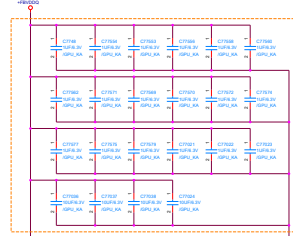
[www.teknisi-indonesia.com](http://www.teknisi-indonesia.com)

Channel A

Under DRAM

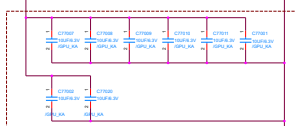


Under DRAM



Around DRAM

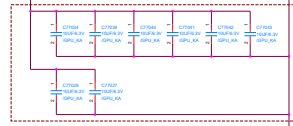
- 22uF x 6pcs
- 10uF x 2pcs



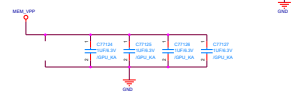
Around DRAM

22uF x 6pcs

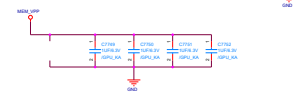
10uF x 2pcs



Under DRAM  
1uF x 4pcs  
4.7uF x 1pcs

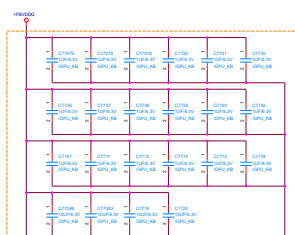


Under DRAM  
1uF x 4pcs  
4.7uF x 1pc

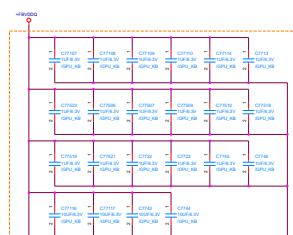


## Channel B

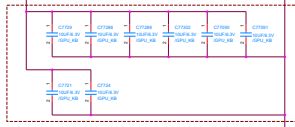
Under DRAM  
1uF x 18pcs  
10uF x 4pcs



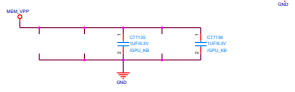
Under DRAM  
1uF x 18pcs  
10uF x 4pcs



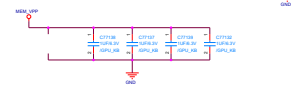
Around DRAM  
22uF x 6pcs  
10uF x 2pcs



Under DRAM  
1uF x 4pcs  
4.7uF x 1pcs

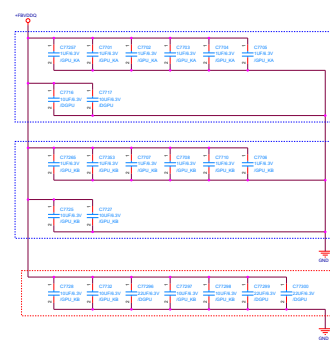


Under DRAM  
1uF x 4pcs  
4.7uF x 1pc



## FBVDDQ (GPU)

Partition A  
Under GPU  
1uF x 6pcs  
10uF x 2pcs



Close GPU  
10uF x 2pcs  
22uF x 5pcs

FBVDDQ (GPU side) <sup>1</sup>	1.35V 1.5V	24 x 0.47uF (0201W X6S) 4 x 10uF (0603 X6S)	2 x 10uF (0603 X6S) <sup>2</sup> 5 x 22uF (0603 X6S)
----- Alternate solution: 12 x 1uF (0402 or 0201W, X6S) <sup>3</sup> 4 x 10uF (0603 X6S)			

Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size <sup>NOTE 1</sup> ]	Quantity	Placement
<b>VDD/VDDQ Rail</b>			
0.47 uF <sup>NOTE 2</sup>	X6S [0201W]	36	Under or very close to DRAM
10 uF	X6S [0603]	4	Around DRAM
10 uF	X6S [0603]	2	
22 uF	X6S [0603]	6	
<b>VPP Rail</b>			
0.47 uF <sup>NOTE 3</sup>	X6S [0201W]	4	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

**For power sequence measurement**



20200319 edition removed. JLG701 follows JCF 890. 04-2014

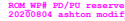
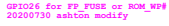
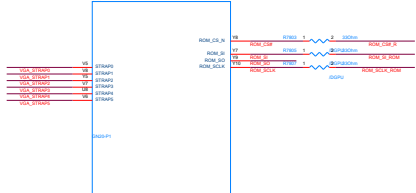


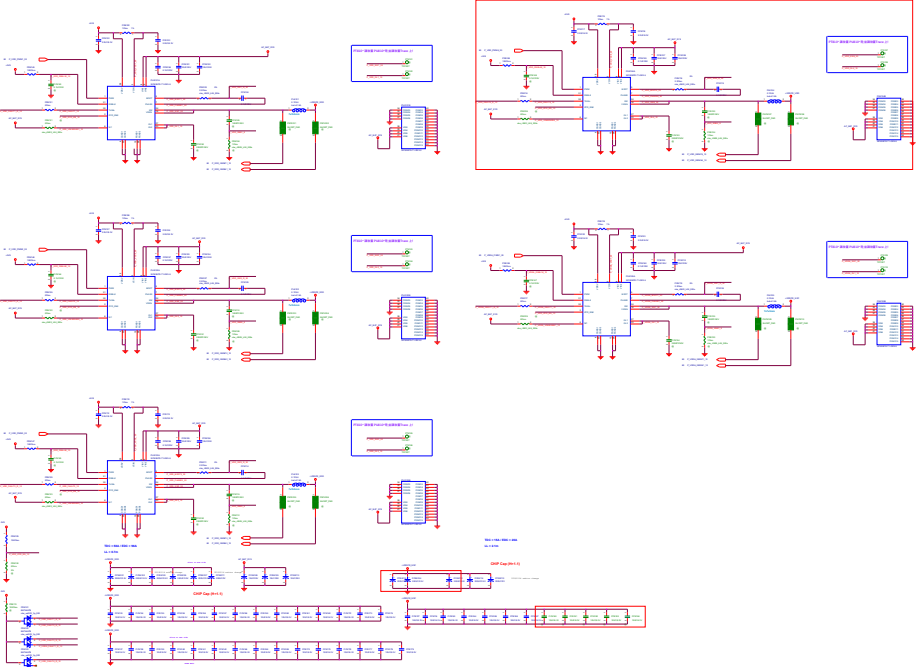
Figure 1 consists of two schematic diagrams. The left diagram is the transmitter, and the right diagram is the receiver. Both are implemented in a 28-nm CMOS technology.

**Transmitter (Left):** A 100-GHz LO signal is input at the top. It splits into two paths. The first path goes through a 100-GHz coupler and a 100-GHz filter to a 100-GHz mixer. The second path goes through a 100-GHz coupler and a 100-GHz filter to a 100-GHz mixer. The two mixers are connected to a 100-GHz coupler and a 100-GHz filter. The output is a 100-GHz signal.

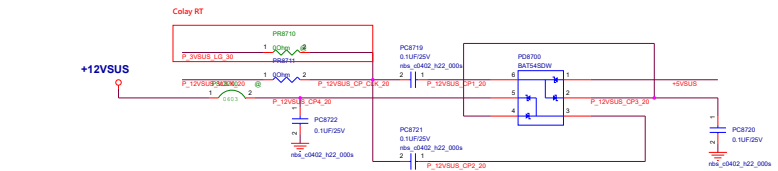
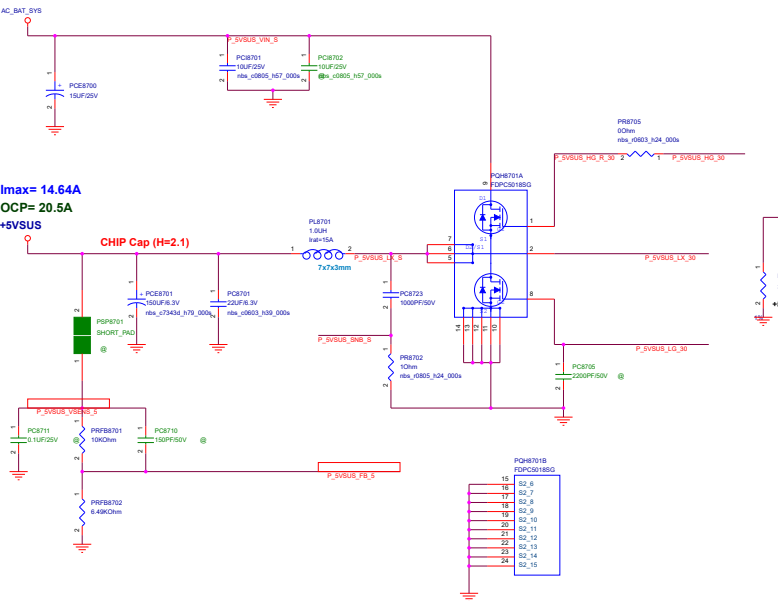
**Receiver (Right):** A 100-GHz LO signal is input at the top. It splits into two paths. The first path goes through a 100-GHz coupler and a 100-GHz filter to a 100-GHz mixer. The second path goes through a 100-GHz coupler and a 100-GHz filter to a 100-GHz mixer. The two mixers are connected to a 100-GHz coupler and a 100-GHz filter. The output is a 100-GHz signal.







CHIP Cap (H=2.1)



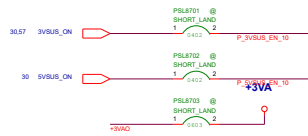
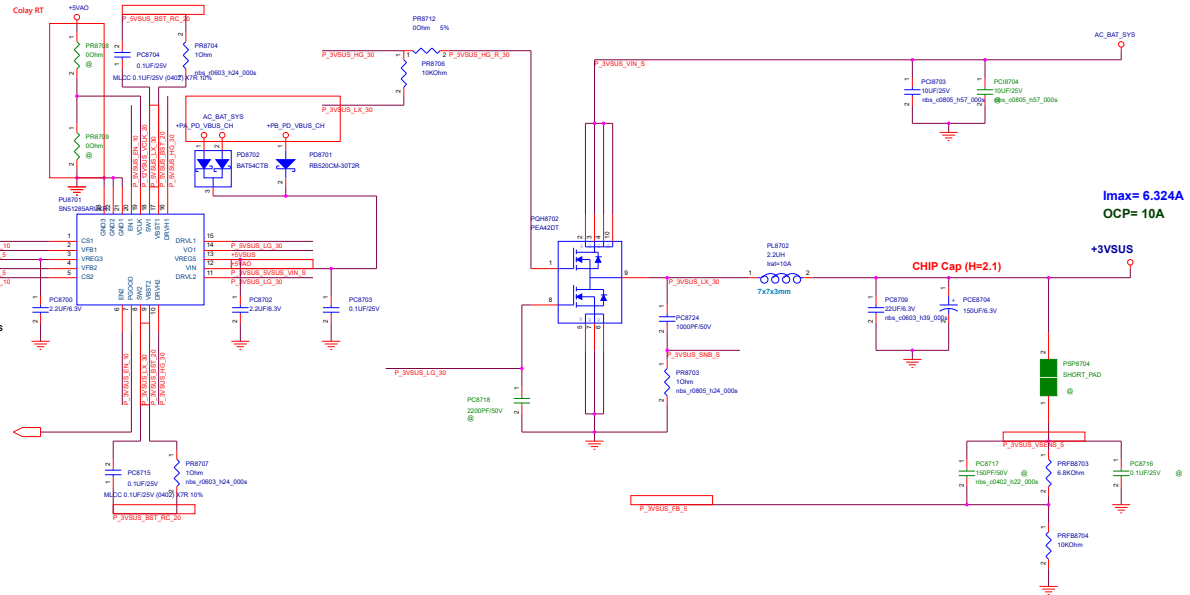
請 检查 整份线路 +12VSUS total 並聯對地電阻不得小於10kOhm

Adaptor Mode (IMVP8)

	S0	S3	S3	D33	S4	S5	SS with USB Charge+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_ECP	1	-	1	-	0	-	0
SUSB_ECP	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	S3	S3	D33	S4	S5	SS with USB Charge+
PS_ON	1	-	1	-	1	0	1
3VADSW_ON	1	-	1	-	1	0	0
5VSUS_ON	1	-	0	0	0	0	0
5VSUS_ON	1	-	0	0	1	0	1
1.35V_ON	1	-	0	0	1	0	0
SUSC_ECP	1	-	0	0	0	0	0
SUSB_ECP	1	-	0	0	0	0	0



PT870\* 請放置 PU8700旁,並請放置Trace 上!





GV301QH SKU Table

Part Number	PCB	SKU	CPU	LPTDR4X	VRAM	PD ID	
60NB06C0-MB621A	R2.0	GV301QH MB_32G/R9-5980B8//R2.0 (V4G)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB4110	R2.0	GV301QH MB_16G/R9-5980B8//R2.0 (V4G)	R9-5980B8	16GB	V4G	WW	
60NB06C0-MB6010	R2.0	GV301QH MB_8G/R9-5980B8//R2.0 (V4G)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB521A	R2.0	GV301QH MB_32G/R9-5900B8//R2.0 (V4G)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB511A	R2.0	GV301QH MB_16G/R9-5900B8//R2.0 (V4G)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB5010	R2.0	GV301QH MB_8G/R9-5900B8//R2.0 (V4G)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB423A	R2.0	GV301QH MB_32G/R7-5800B8//R2.0 (V4G)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB4110	R2.0	GV301QH MB_16G/R7-5800B8//R2.0 (V4G)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB401A	R2.0	GV301QH MB_8G/R7-5800B8//R2.0 (V4G)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MBCC10	R2.0	GV301QH MB_32G/R9-5980B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MBCL10	R2.0	GV301QH MB_16G/R9-5980B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MBCC010	R2.0	GV301QH MB_8G/R9-5980B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB8210	R2.0	GV301QH MB_32G/R9-5900B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB8110	R2.0	GV301QH MB_16G/R9-5900B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB8010	R2.0	GV301QH MB_8G/R9-5900B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB8210	R2.0	GV301QH MB_32G/R7-5800B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB8110	R2.0	GV301QH MB_16G/R7-5800B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	
60NB06C0-MB8010	R2.0	GV301QH MB_8G/R7-5800B8//R2.0 (V4G) (GE)	R9-5980B8	32GB	V4G	WW	

N-KEY

	Win7+ 128GB	128GB
R3104	?	100212000004010
R3106	100212000004010	?
R3107	?	100212000004010
R3108	100212000004010	?
R3164	?	100212000004010
R3174	?	100212100314010
R3209	?	100212100314010
R3211	?	07005-01302000
Q3502	?	
Q3503	?	